THS6212 Differential Broadband PLC Line Driver Amplifier

1 Features

- Low Power Consumption:
  - Full-Bias Mode: 23 mA
  - Mid-Bias Mode: 17.7 mA
  - Low-Bias Mode: 12.2 mA
  - Low-Power Shutdown Mode
  - IADJ Pin for Variable Bias
- Low Noise:
  - Voltage Noise: 2.7 nV/$\sqrt{Hz}$
  - Inverting Current Noise: 17 pA/$\sqrt{Hz}$
  - Noninverting Current Noise: 1.2 pA/$\sqrt{Hz}$
- Low Distortion:
  - –100-dBc HD2 (1-MHz,100-Ω Differential Load)
  - –89-dBc HD3 (1-MHz, 100-Ω Differential Load)
- High Output Current: > 416 mA (25-Ω Load)
- Wide Output Swing: 43.2 V_{PP} (±12-V, 100-Ω Differential Load)
- Wide Bandwidth: 150 MHz (G_{DIFF} = 10 V/V)
- PSRR: 50 dB at 1 MHz for Good Isolation
- Wide Power-Supply Range: 10 V to 28 V

2 Applications

- High Voltage, High Current Driving
- Wide-Band, Power-Line Communications

3 Description

The THS6212 is a differential line-driver amplifier with a current-feedback architecture. The device is targeted for use in broadband, wideband power line communications (PLC) line driver applications and is fast enough to support transmissions of 14.5-dBm line power up to 30 MHz.

The unique architecture of the THS6212 uses minimal quiescent current and still achieves very high linearity. Differential distortion under full bias conditions is –93 dBc at 1 MHz and reduces to only –73 dBc at 10 MHz. Fixed multiple bias settings of the amplifiers allow for enhanced power savings for line lengths where the full performance of the amplifier is not required. To allow for even more flexibility and power savings, an adjustable current pin (IADJ) is available to further lower the bias currents.

The wide output swing of 43.2 V_{PP} (100-Ω differential load) with ±12-V power supplies, coupled with over a 416-mA current drive (25-Ω load), allows for wide dynamic headroom that keeps distortion minimal.

The THS6212 is available in a 24-pin VQFN package and a 17 bond pad wafer sale package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
THS6212	VQFN (24)	5.00 mm × 4.00 mm
THS6212	Wafer sale (17)	2053.00 µm × 1877.00 µm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Line-Driver Circuit Using the THS6212

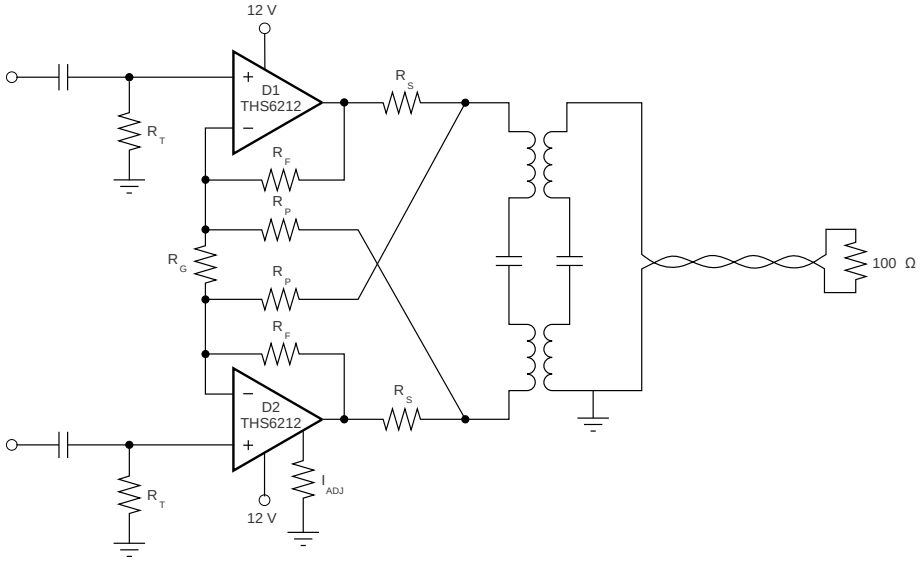


Table of Contents

4 Revision History

Changes from Revision B (May 2018) to Revision C — **Page**

- Added YS bond pad package to document ... 1
- Added YS die package and *Bond Pad Functions* table ... 5
- Added *Wafer and Die Information* section ... 39

Changes from Revision A (March 2017) to Revision B — **Page**

- Changed full-bias mode value from 21 mA to 23 mA in *Features* list ... 1
- Changed mid-bias mode value from 16.2 mA to 17.7 mA in *Features* list ... 1
- Changed low-bias mode value from 11.2 mA to 12.2 mA in *Features* list ... 1
- Added "With Exposed Thermal Pad" to pinout drawing description to *Pin Configuration and Functions* section ... 4
- Deleted I_{S+} quiescent current "T_A = –40°C to +85°C" test conditions and values from *Electrical Characteristics: V_S = ±12 V* table ... 8
- Deleted minimum and maximum full bias I_{S+} quiescent current values from *Electrical Characteristics: V_S = ±12 V* table ... 8
- Changed typical full bias I_{S+} quiescent current value from 21 mA to 23 mA in *Electrical Characteristics: V_S = ±12 V* table. 8
- Deleted minimum and maximum mid bias I_{S+} quiescent current values from *Electrical Characteristics: V_S = ±12 V* table ... 8
- Changed typical mid bias I_{S+} quiescent current value from 16.2 mA to 17.7 mA in *Electrical Characteristics: V_S = ±12 V* table ... 8
- Deleted minimum and maximum low bias I_{S+} quiescent current values from *Electrical Characteristics: V_S = ±12 V* table ... 8
- Changed typical low bias I_{S+} quiescent current value from 11.2 mA to 12.2 mA in *Electrical Characteristics: V_S = ±12 V* table ... 8
- Deleted $I_{S–}$ quiescent current "T_A = –40°C to +85°C" test conditions and values from *Electrical Characteristics: V_S = ±12 V* table ... 8
- Deleted minimum and maximum full bias $I_{S–}$ quiescent current values ... 8
- Changed typical full bias $I_{S–}$ quiescent current value from 20 mA to 22 mA ... 8

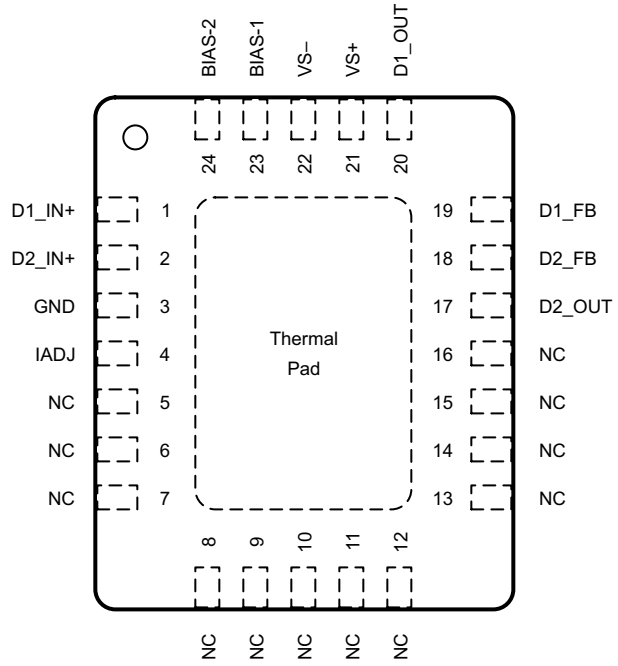
- Deleted minimum and maximum mid bias I_{S-} quiescent current values from *Electrical Characteristics: V_S = ±12 V* table... 8
- Changed typical mid bias I_{S-} quiescent current value from 15.2 mA to 16.7 mA in *Electrical Characteristics: V_S = ±12 V* table ... 8
- Deleted minimum and maximum low bias I_{S-} quiescent current values from *Electrical Characteristics: V_S = ±12 V* table ... 8
- Changed typical low bias I_{S-} quiescent current value from 10.2 mA to 11.2 mA in *Electrical Characteristics: V_S = ±12 V* table... 8
- Deleted I_{S+} quiescent current "T_A = –40°C to +85°C" test conditions and values from *Electrical Characteristics: V_S = 6 V* table ... 11
- Deleted minimum and maximum full bias I_{S+} quiescent current values from *Electrical Characteristics: V_S = 6 V* table..... 11
- Changed typical full bias I_{S+} quiescent current value from 17 mA to 18.6 mA in *Electrical Characteristics: V_S = 6 V* table 11
- Deleted minimum mid bias I_{S+} quiescent current value from *Electrical Characteristics: V_S = 6 V* table ... 11
- Changed typical mid bias I_{S+} quiescent current value from 13.2 mA to 14.4 mA in *Electrical Characteristics: V_S = 6 V* table ... 11
- Deleted minimum and maximum low bias I_{S+} quiescent current values from *Electrical Characteristics: V_S = 6 V* table..... 11
- Changed typical low bias I_{S+} quiescent current value from 9.4 mA to 10.2 mA in *Electrical Characteristics: V_S = 6 V* table ... 11
- Deleted I_{S-} quiescent current "T_A = –40°C to +85°C" test conditions and values from *Electrical Characteristics: V_S = 6 V* table ... 11
- Deleted minimum and maximum full bias I_{S-} quiescent current values from *Electrical Characteristics: V_S = 6 V* table..... 11
- Changed typical full bias I_{S-} quiescent current value from 16 mA to 17.6 mA in *Electrical Characteristics: V_S = 6 V* table 11
- Deleted minimum and maximum mid bias I_{S-} quiescent current values from *Electrical Characteristics: V_S = 6 V* table..... 11
- Changed typical full bias I_{S-} quiescent current value from 12.2 mA to 13.4 mA in *Electrical Characteristics: V_S = 6 V* table ... 11
- Deleted minimum and maximum low bias I_{S-} quiescent current values from *Electrical Characteristics: V_S = 6 V* table 11
- Changed typical low bias I_{S-} quiescent current value from 8.4 mA to 9.2 mA in *Electrical Characteristics: V_S = 6 V* table 11
- Changed Quiescent Current for Full Bias Setting vs R_{ADJ} graph ... 14
- Changed Quiescent Current for Mid Bias Setting vs R_{ADJ} graph ... 16
- Changed Supply Current for Low Bias Setting vs R_{ADJ} graph... 18
- Changed Quiescent Current for Full Bias Setting vs R_{ADJ} graph ... 21
- Changed Quiescent Current for Mid Bias Setting vs R_{ADJ} graph ... 23
- Changed Quiescent Current for Low Bias Setting vs R_{ADJ} graph ... 25
- Changed quiescent current value from 21 mA to 23 mA in *Wideband Current-Feedback Operation* section... 31
- Changed quiescent current value from 21 mA to 23 mA in paragraph above Equation 19... 37
- Changed 21 mA to 23 mA and 955 mW to 1003 mW in Equation 19... 37
- Changed *Board Layout Guidelines* section title to *Layout Guidelines* to align with standards ... 38

Changes from Original (May 2016) to Revision A **Page**

- Changed document title from *THS6212 Differential, Line-Driver Amplifier* to *THS6212 Differential Broadband PLC Line Driver Amplifier* ... 1
- Changed *line-driver applications (such as wide-band, power-line communications)* to *broadband and wideband power line communications (PLC) line driver applications* in second sentence of *Description* section ... 1

5 Pin Configuration and Functions

RHF Package
24-Pin VQFN With Exposed Thermal Pad
Top View



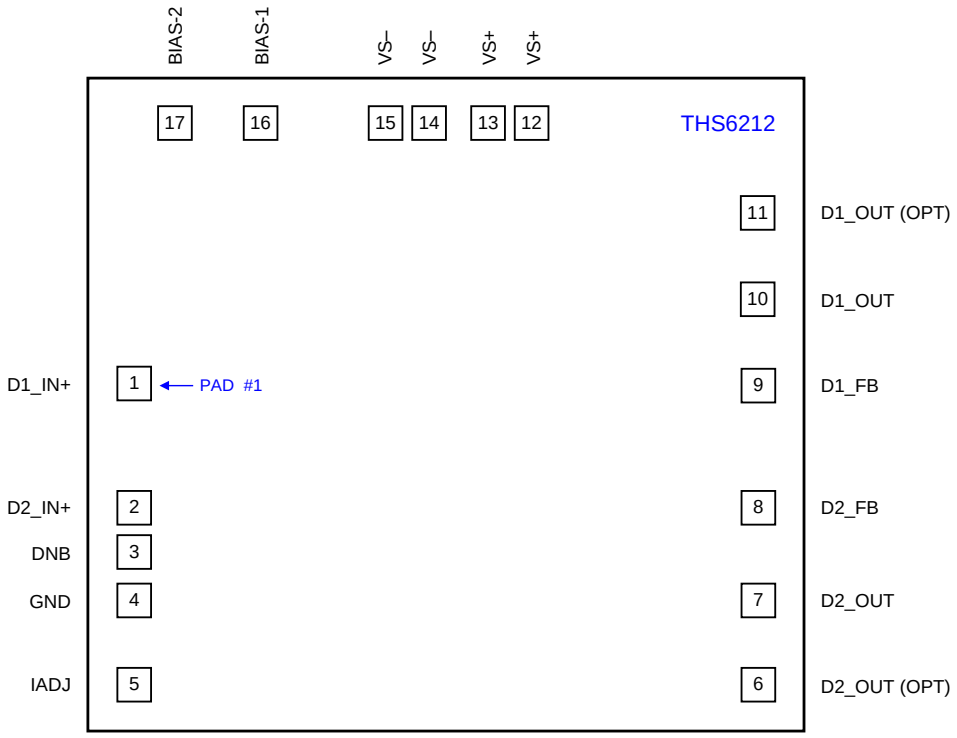
NOTE: NC = no internal connection.

Pin Functions[1]

PIN		I/O	DESCRIPTION
NAME	NO.		
BIAS-1	23	I	Bias mode parallel control, LSB
BIAS-2	24	I	Bias mode parallel control, MSB
D1_FB	19	I	Amplifier D1 inverting input
D2_FB	18	I	Amplifier D2 inverting input
D1_IN+	1	I	Amplifier D1 noninverting input
D2_IN+	2	I	Amplifier D2 noninverting input
D1_OUT	20	O	Amplifier D1 output
D2_OUT	17	O	Amplifier D2 output
GND[2]	3	I/O	Control pin ground reference
IADJ	4	I/O	Bias current adjustment pin
NC	5-16	—	No internal connection
VS–	22	I/O	Negative power-supply connection
VS+	21	I/O	Positive power-supply connection

(1) The THS6212 defaults to the shutdown (disable) state if a signal is not present on the bias pins.
(2) The GND pin ranges from VS– to (VS+ – 5 V).

YS Die
17-Pad Wafer Sale
Top View



NOTE: DNB = do not bond.

Bond Pad Functions

PAD		I/O	DESCRIPTION
NAME	NO.		
BIAS-1 (1)	16	I	Bias mode parallel control, LSB
BIAS-2 (1)	17	I	Bias mode parallel control, MSB
D1_FB	9	I	Amplifier D1 inverting input
D1_IN+	1	I	Amplifier D1 noninverting input
D2_IN+	2	I	Amplifier D2 noninverting input
D1_OUT	10	O	Amplifier D1 output (must be used for D1 output)
D1_OUT (OPT)	11	O	Optional amplifier D1 output (pad can be left unconnected or connected to pad 10)
D2_FB	8	I	Amplifier D2 inverting input
D2_OUT (OPT)	6	O	Optional amplifier D2 output (can be left unconnected or connected to pad 7)
D2_OUT	7	O	Amplifier D2 output (must be used for D2 output)
DNB	3	—	Do not bond (for internal use)
GND (2)	4	I/O	Control pin ground reference
IADJ	5	I/O	Bias current adjustment pin
VS–	14, 15	I/O	Negative power-supply connection
VS+	12, 13	I/O	Positive power-supply connection
Backside	—	—	Dielectrically isolated, no internal connection, can be floating or connected to any potential inclusive of and in between VS+ and VS– (must be connected to a thermally dissipating element)

(1) The THS6212 defaults to the shutdown (disable) state if a signal is not present on the bias pins.
(2) The GND pin ranges from VS– to (VS+ – 5 V).

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, $V_{S–}$ to V_{S+}			28	V
Input voltage, V_I			$\pm V_S$	V
Differential input voltage, V_{ID}			±2	V
Output current, I_O	Static DC(2)		±500	mA
Continuous power dissipation		See *Thermal Information* table		
Maximum junction temperature, T_J	Under any condition(3)		150	°C
	Continuous operation, long-term reliability(4)		130	
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The THS6212 incorporates a thermal pad on the underside of the device. This pad functions as a heatsink and must be connected to a thermally dissipating plane for proper power dissipation. Failure to do so can result in exceeding the maximum junction temperature, which can permanently damage the device.
(3) The absolute maximum junction temperature under any condition is limited by the constraints of the silicon process.
(4) The absolute maximum junction temperature for continuous operation is limited by the package constraints. Operation above this temperature can result in reduced reliability or lifetime of the device.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	
		Machine model (MM)	±100	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Supply voltage, $V_{S–}$ to V_{S+}	10		28	V
T_J	Operating junction temperature			130	°C
T_A	Ambient operating air temperature		25	85	°C

6.4 Thermal Information

THERMAL METRIC(1)		THS6212 RHF (VQFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	31.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics: V_S = ±12 V

at T_A = 25°C, G_{DIFF} = 10 V/V with R_L = 100-Ω differential load, R_{ADJ} = 0 Ω, and full bias (unless otherwise noted); see Figure 81 for setup

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	TEST LEVEL(1)
AC PERFORMANCE								
SSBW	Small-signal bandwidth, –3 dB	G_{DIFF} = 5 V/V , R_F = 1.5 kΩ, V_O = 2 V_{PP}			160		MHz	C
		G_{DIFF} = 10 V/V , R_F = 1.24 kΩ, V_O = 2 V_{PP}		120	150			B
		T_A = –40°C to +85°C		100				
	0.1-dB bandwidth flatness	G_{DIFF} = 10 V/V , R_F = 1.24 kΩ			114		MHz	C
LSBW	Large-signal bandwidth	G_{DIFF} = 10 V/V , R_F = 1.24 kΩ, V_O = 20 V_{PP}			120		MHz	C
SR	Slew rate (10% to 90% level)	G_{DIFF} = 10 V/V, V_O = 20-V step, differential		3200	3800		V/µs	B
		T_A = –40°C to +85°C		3000				B
	Rise and fall time	G_{DIFF} = 10 V/V, V_O = 2 V_{PP}			5		ns	C
HD2	2nd-order harmonic distortion	G_{DIFF} = 10 V/V, V_O = 2 V_{PP}, R_L = 100-Ω differential	Full bias, f = 1 MHz		–100	–95	dBc	B
			T_A = –40°C to +85°C			–90		B
			Low bias, f = 1 MHz		–96			C
			Full bias, f = 10 MHz		–75	–70		B
			T_A = –40°C to +85°C			–65		B
			Low bias, f = 10 MHz		–72			C
HD3	3rd-order harmonic distortion	G_{DIFF} = 10 V/V, V_O = 2 V_{PP}, R_L = 100-Ω differential	Full bias, f = 1 MHz		–89	–85	dBc	B
			T_A = –40°C to +85°C			–80		B
			Low bias, f = 1 MHz		–85			C
			Full bias, f = 10 MHz		–73	–65		B
			T_A = –40°C to +85°C			–53		B
			Low bias, f = 10 MHz		–58			C
e_n	Differential input voltage noise	f = 1 MHz, input-referred			2.7	3.2	nV/√Hz	B
		T_A = –40°C to +85°C				3.5		B
i_{n+}	Differential noninverting current noise	f = 1 MHz			1.2	1.4	pA/√Hz	B
		T_A = –40°C to +85°C				1.6		B
i_{n-}	Differential inverting current noise	f = 1 MHz			17	20	pA/√Hz	B
		T_A = –40°C to +85°C				24		B
DC PERFORMANCE								
Z_{OL}	Open-loop transimpedance gain	R_L = 100 Ω		330	700		kΩ	A
				300				B
	Input offset voltage				±15	±50	mV	A
		T_A = –40°C to +85°C				±60		B
	Input offset voltage drift	T_A = –40°C to +85°C				±155	µV/°C	B
	Input offset voltage matching				±0.5	±5	mV	A
		T_A = –40°C to +85°C				±7		B
	Noninverting input bias current				±1	±3.5	µA	A
		T_A = –40°C to +85°C				±5.5		B
	Noninverting input bias current drift	T_A = –40°C to +85°C				±30	nA/°C	B
	Inverting input bias current				±8	±45	µA	A
		T_A = –40°C to +85°C				±55		B
	Inverting input bias current drift	T_A = –40°C to +85°C				±154	nA/°C	B
	Inverting input bias current matching				±8	±30	µA	A
		T_A = –40°C to +85°C				±40		B

(1) Test levels: (A) 100% tested at 25°C. Overtemperature limits set by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.

Electrical Characteristics: V_S = ±12 V (continued)

at T_A = 25°C, G_{DIFF} = 10 V/V with R_L = 100-Ω differential load, R_{ADJ} = 0 Ω, and full bias (unless otherwise noted); see Figure 81 for setup

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL (1)
INPUT CHARACTERISTICS							
	Common-mode input range	Each input	±9	±9.5		V	A
		T_A = –40°C to +85°C	±8.6				B
CMRR	Common-mode rejection ratio	Each input	53	65		dB	A
		T_A = –40°C to +85°C	49				B
	Noninverting input resistance			500 || 2		kΩ || pF	C
	Inverting input resistance			50		Ω	C
OUTPUT CHARACTERISTICS							
	Output voltage swing	R_L = 100 Ω, each output		±10.9		V	C
		R_L = 50 Ω, each output	±10.6	±10.8			A
		T_A = –40°C to +85°C	±10.4				B
		R_L = 25 Ω, each output	±10.2	±10.4			A
		T_A = –40°C to +85°C	±10				B
	Output current (sourcing and sinking)	R_L = 25 Ω, based on V_O tests	±408	±416		mA	A
		T_A = –40°C to +85°C	±400				B
	Short-circuit output current			1		A	C
z_o	Output impedance	f = 1 MHz, differential		0.2		Ω	C
	Crosstalk	f = 1 MHz, V_O = 2 V_{PP}, port 1 to port 2		–90		dB	C
POWER SUPPLY							
V_S	Operating voltage		±5	±12	±14	V	A
		T_A = –40°C to +85°C	±5		±14		C
	I_{S+} quiescent current	Full bias (BIAS-1 = 0, BIAS-2 = 0)		23		mA	A
		Mid bias (BIAS-1 = 1, BIAS-2 = 0)		17.7			A
		Low bias (BIAS-1 = 0, BIAS-2 = 1)		12.2			A
		Bias off (BIAS-1 = 1, BIAS-2 = 1)		0.4	0.8	mA	A
	$I_{S–}$ quiescent current	Full bias (BIAS-1 = 0, BIAS-2 = 0)		22		mA	A
		Mid bias (BIAS-1 = 1, BIAS-2 = 0)		16.7			A
		Low bias (BIAS-1 = 0, BIAS-2 = 1)		11.2			A
		Bias off (BIAS-1 = 1, BIAS-2 = 1)		0.1	0.3	mA	A
	Current through GND pin	Full bias (BIAS-1 = 0, BIAS-2 = 0)		1		mA	C
+PSRR	Positive power-supply rejection ratio	Differential	54	66		dB	A
		T_A = –40°C to +85°C	52				B
–PSRR	Negative power-supply rejection ratio	Differential	52	65		dB	A
		T_A = –40°C to +85°C	50				B

Electrical Characteristics: V_S = ±12 V (continued)

at T_A = 25°C, G_{DIFF} = 10 V/V with R_L = 100-Ω differential load, R_{ADJ} = 0 Ω, and full bias (unless otherwise noted); see Figure 81 for setup

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(1)
BIAS CONTROL						
Bias control pin logic threshold	Logic 1, with respect to GND(2), T_A = –40°C to +85°C	1.9			V	B
	Logic 0, with respect to GND(2), T_A = –40°C to +85°C			0.8		B
Bias control pin quiescent current	BIAS-1, BIAS-2 = 0.5 V (logic 0)		20	30	µA	A
	T_A = –40°C to +85°C			35		B
	BIAS-1, BIAS-2 = 3.3 V (logic 1)		0.3	1		A
	T_A = –40°C to +85°C			1.2		B
Bias pin input impedance			50		kΩ	C
Amplifier output impedance	Off bias (BIAS-1 = 1, BIAS-2 = 1)		10 || 5		kΩ || pF	C

(2) The GND pin usable range is from $V_{S–}$ to (V_{S+} – 5 V).

6.6 Electrical Characteristics: V_S = ±6 V

at T_A = 25°C, G_{DIFF} = 5 V/V with R_L = 100-Ω differential load, R_{ADJ} = 0 Ω, and full bias (unless otherwise noted); see Figure 81 for setup

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	TEST LEVEL(1)
AC PERFORMANCE								
SSBW	Small-signal bandwidth, –3 dB	G_{DIFF} = 5 V/V , R_F = 1.82 kΩ, V_O = 2 V_{PP}			140		MHz	C
		G_{DIFF} = 10 V/V , R_F = 1.5 kΩ, V_O = 2 V_{PP}		110	140			B
		T_A = –40°C to +85°C		95				
	0.1-dB bandwidth flatness	G_{DIFF} = 5 V/V , R_F = 1.82 kΩ			100		MHz	C
LSBW	Large-signal bandwidth	G_{DIFF} = 5 V/V , R_F = 1.82 kΩ, V_O = 16 V_{PP}			120		MHz	C
SR	Slew rate (10% to 90% level)	G_{DIFF} = 5 V/V, V_O = 10-V step, differential		1200	1600		V/µs	B
		T_A = –40°C to +85°C		1000				B
	Rise and fall time	G_{DIFF} = 5 V/V, V_O = 2 V_{PP}			5		ns	C
HD2	2nd-order harmonic distortion	G_{DIFF} = 5 V/V, V_O = 2 V_{PP}, R_L = 100-Ω differential	Full bias		–98	–92	dBc	B
			T_A = –40°C to +85°C			–87		B
			Low bias		–93			C
			Full bias		–80	–75		B
			T_A = –40°C to +85°C			–68		B
			Low bias		–74			C
HD3	3rd-order harmonic distortion	G_{DIFF} = 5 V/V, V_O = 2 V_{PP}, R_L = 100-Ω differential	Full bias		–93	–84	dBc	B
			T_A = –40°C to +85°C			–79		B
			Low bias		–89			C
			Full bias		–66	–60		B
			T_A = –40°C to +85°C			–54		B
			Low bias		–55			C
e_n	Differential input voltage noise	f = 1 MHz, input-referred			2.5	3.0	nV/√Hz	B
		T_A = –40°C to +85°C				3.3		B
i_{n+}	Differential noninverting current noise	f = 1 MHz			1.2	1.4	pA/√Hz	B
		T_A = –40°C to +85°C				1.6		B
i_{n-}	Differential inverting current noise	f = 1 MHz			17	20	pA/√Hz	B
		T_A = –40°C to +85°C				24		B
DC PERFORMANCE								
Z_{OL}	Open-loop transimpedance gain	R_L = 100 Ω		330	650		kΩ	A
		T_A = –40°C to +85°C		300				B
	Input offset voltage				±10	±45	mV	A
		T_A = –40°C to +85°C				±55		B
	Input offset voltage drift	T_A = –40°C to +85°C				±155	µV/°C	B
	Input offset voltage matching	Channels 1 to 2			±0.5	±5	mV	A
		T_A = –40°C to +85°C				±7		B
	Noninverting input bias current				±1	±3.5	µA	A
		T_A = –40°C to +85°C				±5.5		B
	Noninverting input bias current drift	T_A = –40°C to +85°C				±30	nA/°C	B
	Inverting input bias current				±8	±45	µA	A
		T_A = –40°C to +85°C				±55		B
	Inverting input bias current drift	T_A = –40°C to +85°C				±135	nA/°C	B
	Inverting input bias current matching				±8	±30	µA	A
		T_A = –40°C to +85°C				±40		B

(1) Test levels: (A) 100% tested at 25°C. Overtemperature limits set by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.

Electrical Characteristics: V_S = ±6 V (continued)

at T_A = 25°C, G_{DIFF} = 5 V/V with R_L = 100-Ω differential load, R_{ADJ} = 0 Ω, and full bias (unless otherwise noted); see Figure 81 for setup

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(1)
INPUT CHARACTERISTICS							
	Common-mode input range	Each input	±2.9	±3.0		V	A
		T_A = –40°C to +85°C	±2.7				B
CMRR	Common-mode rejection ratio	Each input	51	62		dB	A
		T_A = –40°C to +85°C	47				B
	Noninverting input resistance			500 || 2		kΩ || pF	C
	Inverting input resistance			55		Ω	C
OUTPUT CHARACTERISTICS							
	Output voltage swing	R_L = 100 Ω, each output		±4.9		V	C
		R_L = 50 Ω, each output	±4.75	±4.9			A
		T_A = –40°C to +85°C	±4.6				B
		R_L = 25 Ω, each output	±4.55	±4.7			A
		T_A = –40°C to +85°C	±4.4				B
	Output current (sourcing and sinking)	R_L = 25 Ω, based on V_O tests	±182	±188		mA	A
		T_A = –40°C to +85°C	±176				B
	Short-circuit output current			±1		A	C
z_o	Output impedance	f = 1 MHz, differential		0.2		Ω	C
	Crosstalk	f = 1 MHz, V_O = 2 V_{PP}, port 1 to port 2		–90		dB	C
POWER SUPPLY							
V_S	Operating voltage		±5	±6	±14	V	A
		T_A = –40°C to +85°C	±5		±14		C
	I_{S+} quiescent current	Full bias (BIAS-1 = 0, BIAS-2 = 0)		18.6		mA	A
		Mid bias (BIAS-1 = 1, BIAS-2 = 0)		14.4			A
		Low bias (BIAS-1 = 0, BIAS-2 = 1)		10.2			A
		Bias off (BIAS-1 = 1, BIAS-2 = 1)		0.5	0.8	mA	A
	$I_{S–}$ quiescent current	Full bias (BIAS-1 = 0, BIAS-2 = 0)		17.6		mA	A
		Mid bias (BIAS-1 = 1, BIAS-2 = 0)		13.4			A
		Low bias (BIAS-1 = 0, BIAS-2 = 1)		9.2			A
		Bias off (BIAS-1 = 1, BIAS-2 = 1)		0.1	0.3		A
	Current through GND pin	Full bias (BIAS-1 = 0, BIAS-2 = 0)		1		mA	C
+PSRR	Positive power-supply rejection ratio	Differential	54	64		dB	A
		T_A = –40°C to +85°C	52				B
–PSRR	Negative power-supply rejection ratio	Differential	52	63		dB	A
		T_A = –40°C to +85°C	50				B

Electrical Characteristics: V_S = ±6 V (continued)

at T_A = 25°C, G_{DIFF} = 5 V/V with R_L = 100-Ω differential load, R_{ADJ} = 0 Ω, and full bias (unless otherwise noted); see Figure 81 for setup

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(1)
BIAS CONTROL						
Bias control pin logic threshold	Logic 1, with respect to GND(2), T_A = –40°C to +85°C	1.9			V	B
	Logic 0, with respect to GND(2), T_A = –40°C to +85°C			0.8		B
Bias control pin quiescent current	BIAS-1, BIAS-2 = 0.5 V (logic 0)		20	30	µA	A
	T_A = –40°C to +85°C			35		B
	BIAS-1, BIAS-2 = 3.3 V (logic 1)		0.3	1		A
	T_A = –40°C to +85°C			1.2		B
Bias pin input impedance			50		kΩ	C
Amplifier output impedance	Off bias (BIAS-1 = 1, BIAS-2 = 1)		10 || 5		kΩ || pF	C

(2) The GND pin usable range is from $V_{S–}$ to (V_{S+} – 5 V).

6.7 Timing Requirements

		MIN	NOM	MAX	UNIT
t_{ON}	Turn-on time delay: time for I_S to reach 50% of final value		1		µs
t_{OFF}	Turn-off time delay: time for I_S to reach 50% of final value		1		µs

6.8 Typical Characteristics: V_S = ±12 V (Full Bias)

at T_A = 25°C, G_{DIFF} = 10 V/V, G_{CM} = 1 V/V, R_{ADJ} = 0 Ω, R_F = 1.24 kΩ, and R_L = 100 Ω (unless otherwise noted)

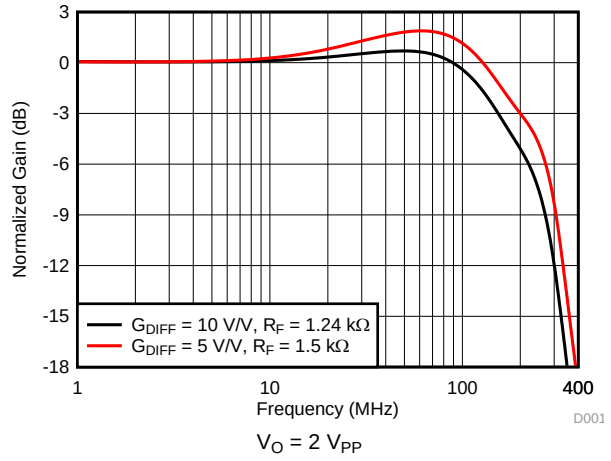


Figure 1. Small-Signal Frequency Response

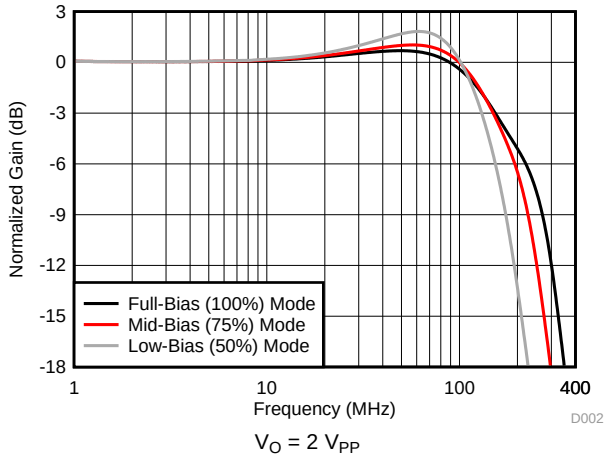


Figure 2. Small-Signal Frequency Response vs Bias Mode

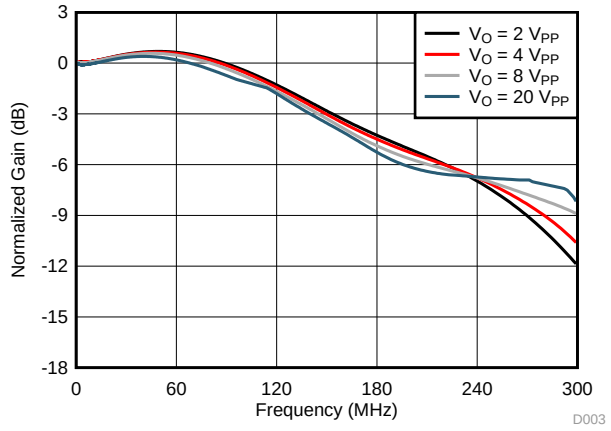


Figure 3. Large-Signal Frequency Response

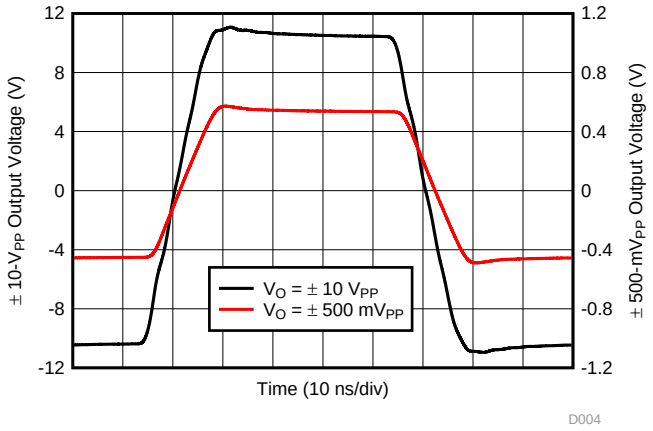


Figure 4. Pulse Response

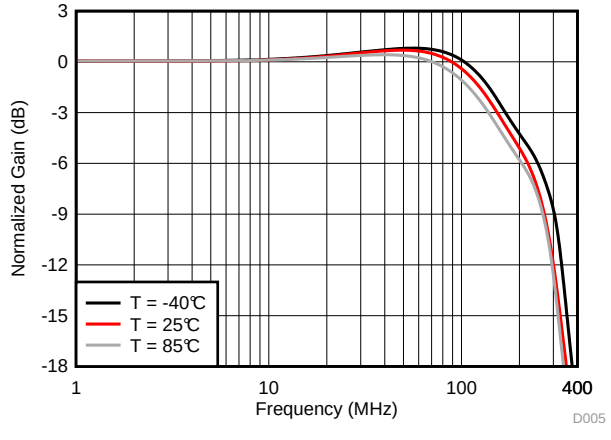


Figure 5. Frequency Response Across Temperature

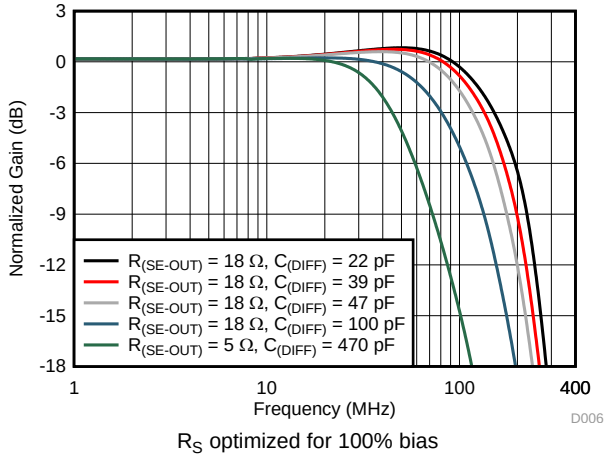
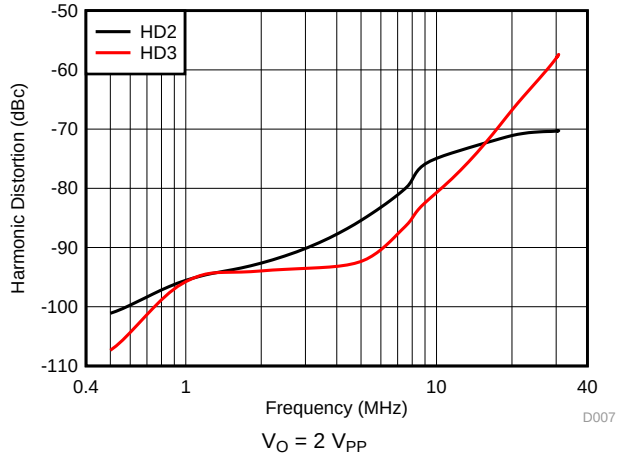


Figure 6. Frequency Response Across Capacitive Load

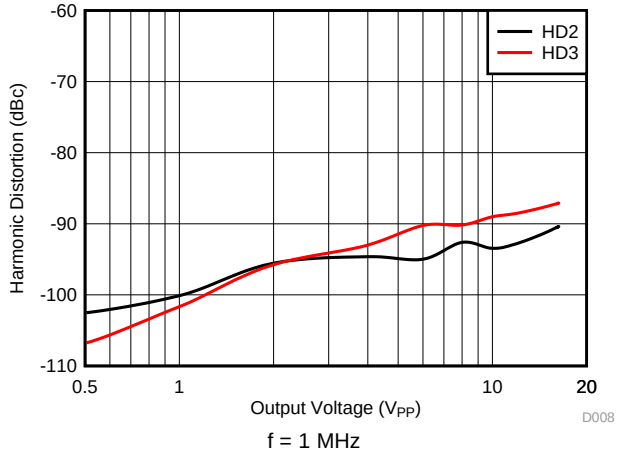
Typical Characteristics: V_S = ±12 V (Full Bias) (continued)

at T_A = 25°C, G_{DIFF} = 10 V/V, G_{CM} = 1 V/V, R_{ADJ} = 0 Ω, R_F = 1.24 kΩ, and R_L = 100 Ω (unless otherwise noted)



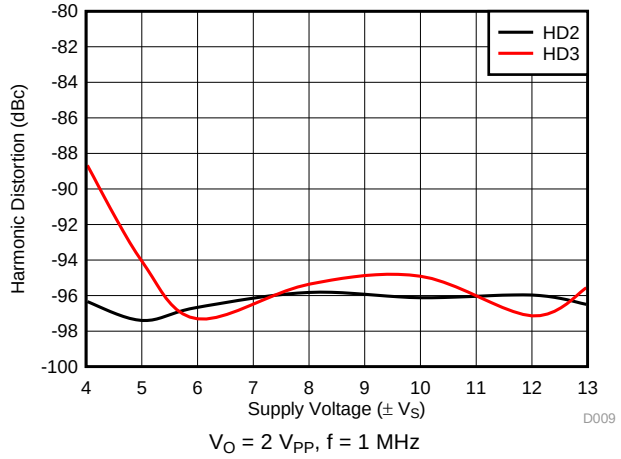
V_O = 2 V_{PP}

Figure 7. Harmonic Distortion vs Frequency



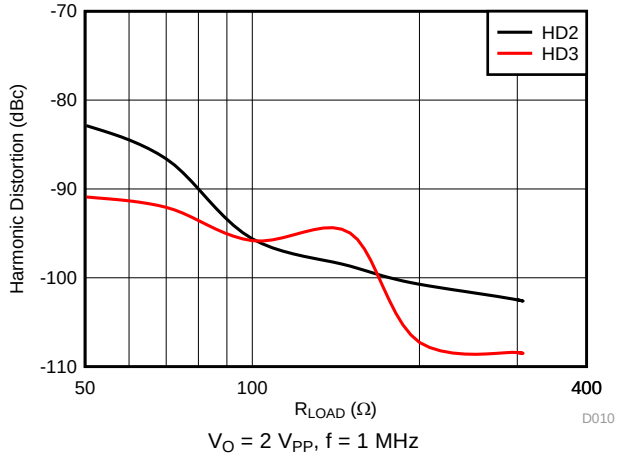
f = 1 MHz

Figure 8. Harmonic Distortion vs Output Voltage



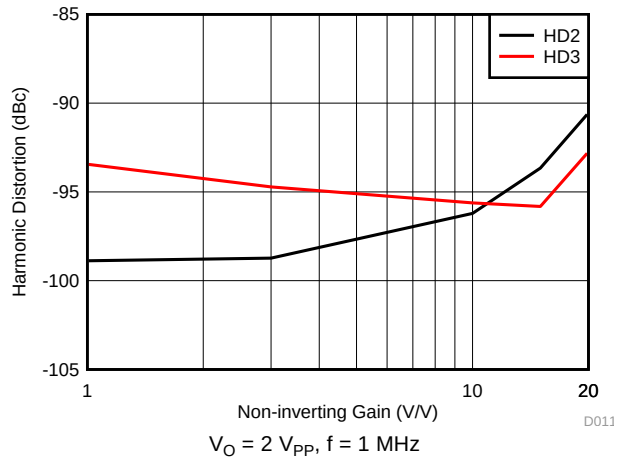
V_O = 2 V_{PP}, f = 1 MHz

Figure 9. Harmonic Distortion vs Supply Voltage



V_O = 2 V_{PP}, f = 1 MHz

Figure 10. Harmonic Distortion vs Load Resistance



V_O = 2 V_{PP}, f = 1 MHz

Figure 11. Harmonic Distortion vs Noninverting Gain

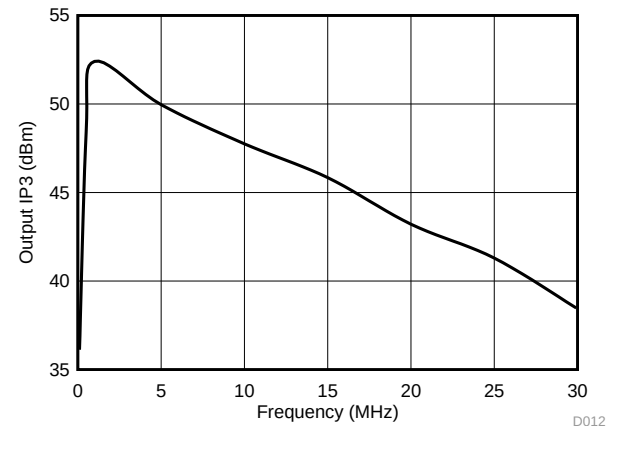


Figure 12. Two-Tone, Third-Order Intermodulation Intercept

Typical Characteristics: V_S = ±12 V (Full Bias) (continued)

at T_A = 25°C, G_{DIFF} = 10 V/V, G_{CM} = 1 V/V, R_{ADJ} = 0 Ω, R_F = 1.24 kΩ, and R_L = 100 Ω (unless otherwise noted)

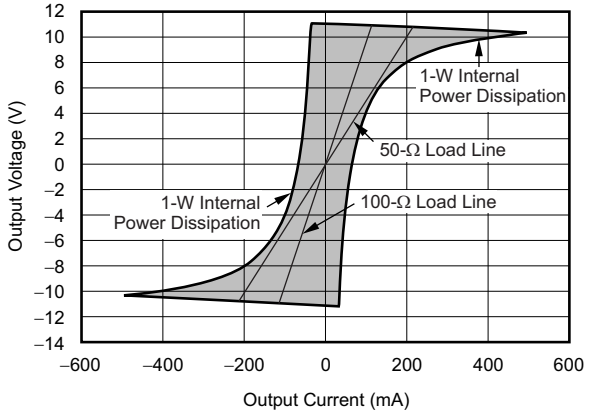
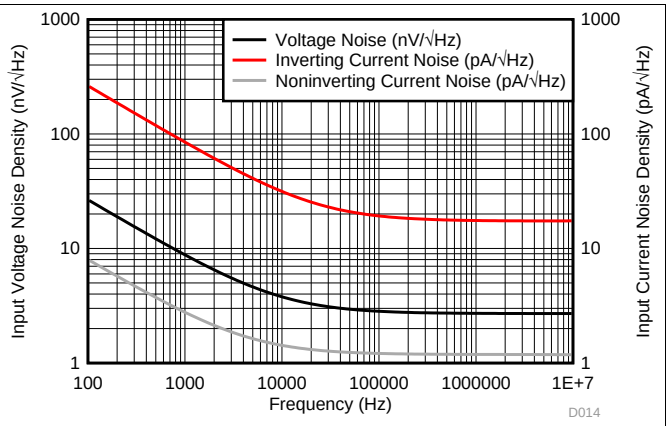


Figure 13. Output Voltage and Current Limitations



Voltage and current noise contributing to differential noise

Figure 14. Input Voltage and Current Noise Density

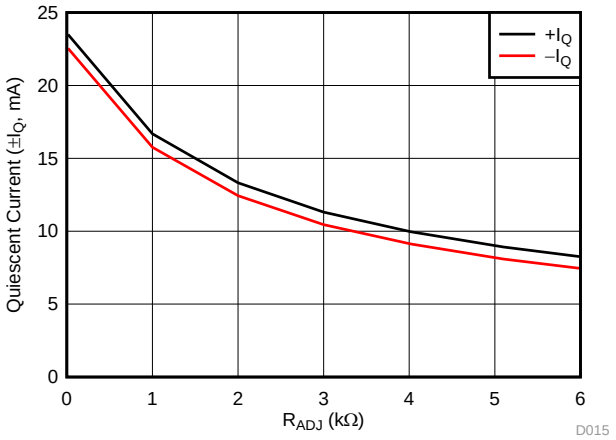


Figure 15. Quiescent Current for Full Bias Setting vs R_{ADJ}

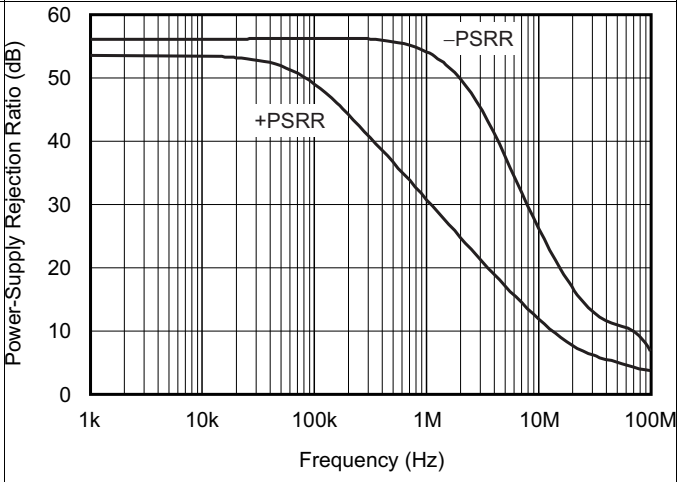


Figure 16. PSRR vs Frequency

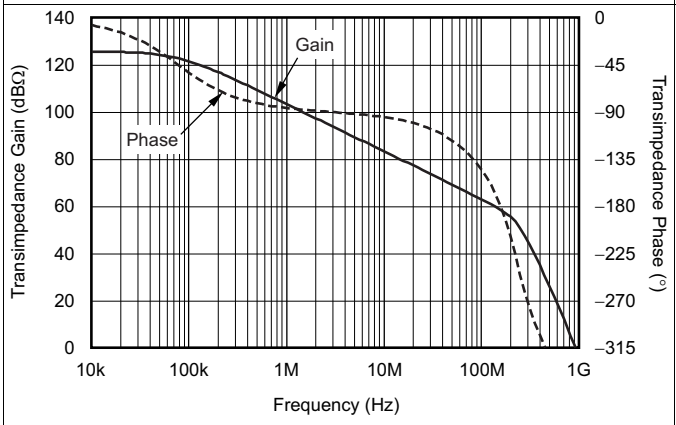


Figure 17. Open-Loop Gain and Phase

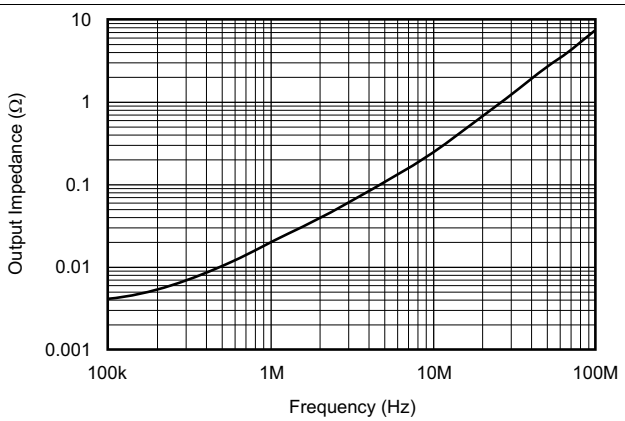
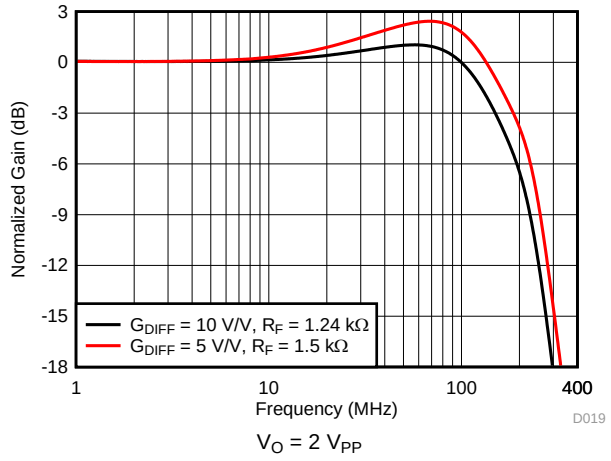


Figure 18. Closed-Loop Output Impedance

6.9 Typical Characteristics: V_S = ±12 V (Mid Bias)

at T_A = 25°C, G_{DIFF} = 10 V/V, G_{CM} = 1 V/V, R_{ADJ} = 0 Ω, R_F = 1.24 kΩ, and R_L = 100 Ω (unless otherwise noted)



V_O = 2 V_{PP}

Figure 19. Small-Signal Frequency Response

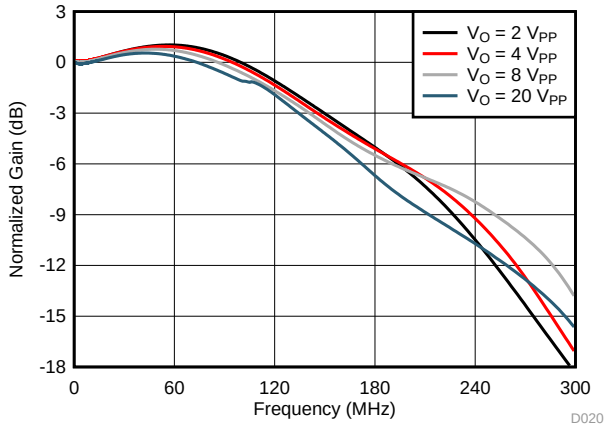


Figure 20. Large-Signal Frequency Response

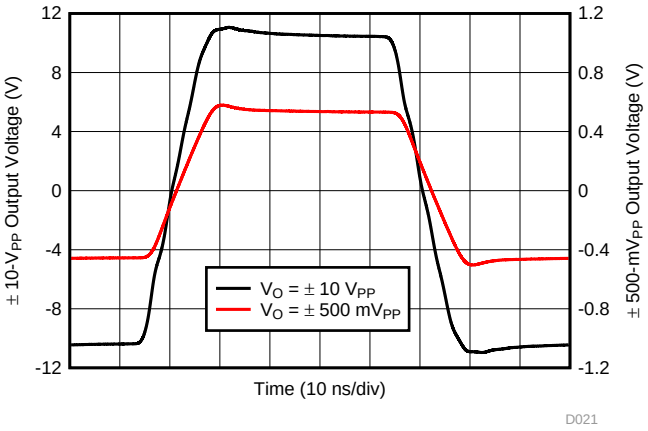


Figure 21. Pulse Response

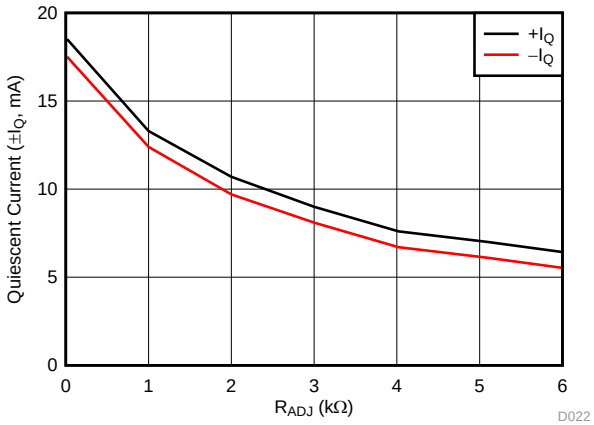


Figure 22. Quiescent Current for Mid Bias Setting vs R_{ADJ}

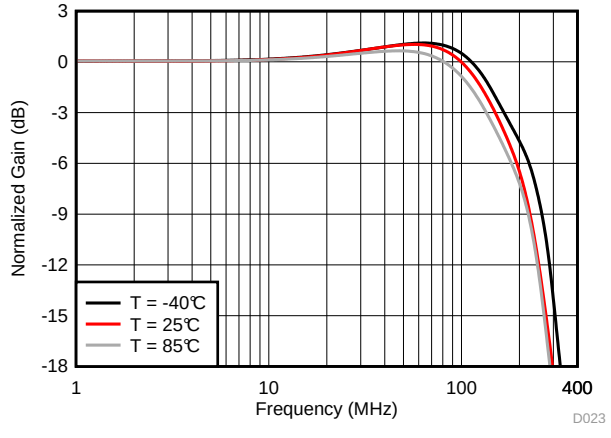
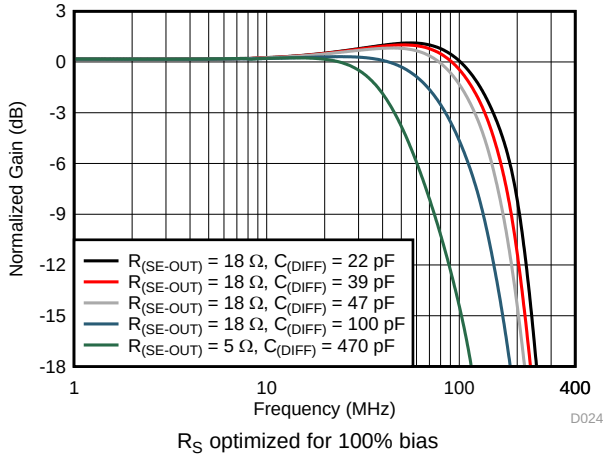


Figure 23. Frequency Response Across Temperature

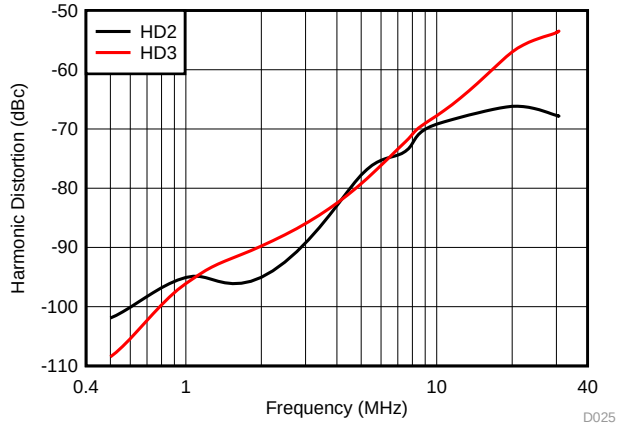


R_S optimized for 100% bias

Figure 24. Frequency Response Across Capacitive Load

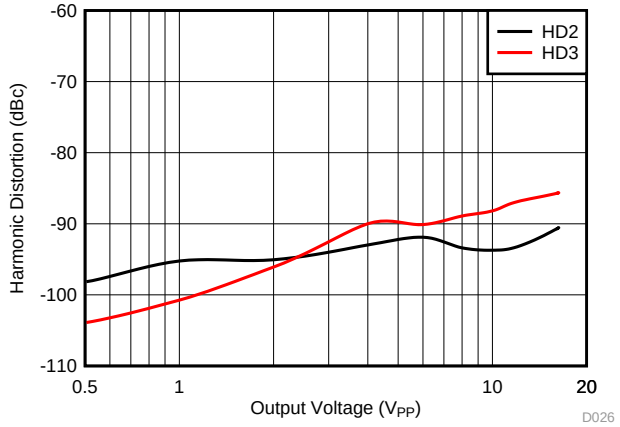
Typical Characteristics: V_S = ±12 V (Mid Bias) (continued)

at T_A = 25°C, G_{DIFF} = 10 V/V, G_{CM} = 1 V/V, R_{ADJ} = 0 Ω, R_F = 1.24 kΩ, and R_L = 100 Ω (unless otherwise noted)



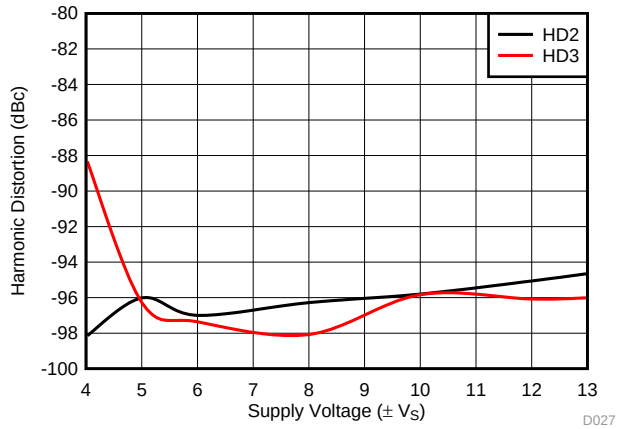
V_O = 2 V_{PP}

Figure 25. Harmonic Distortion vs Frequency



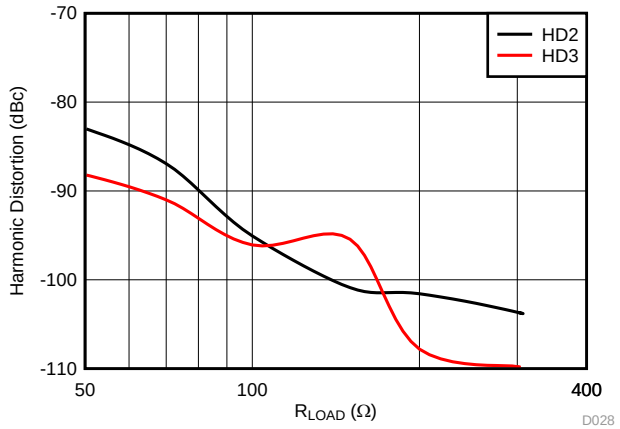
f = 1 MHz

Figure 26. Harmonic Distortion vs Output Voltage



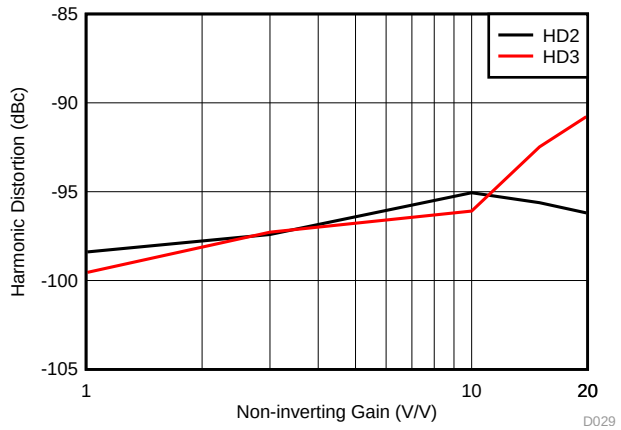
V_O = 2 V_{PP}, f = 1 MHz

Figure 27. Harmonic Distortion vs Supply Voltage



V_O = 2 V_{PP}, f = 1 MHz

Figure 28. Harmonic Distortion vs Load Resistance



V_O = 2 V_{PP}, f = 1 MHz

Figure 29. Harmonic Distortion vs Noninverting Gain

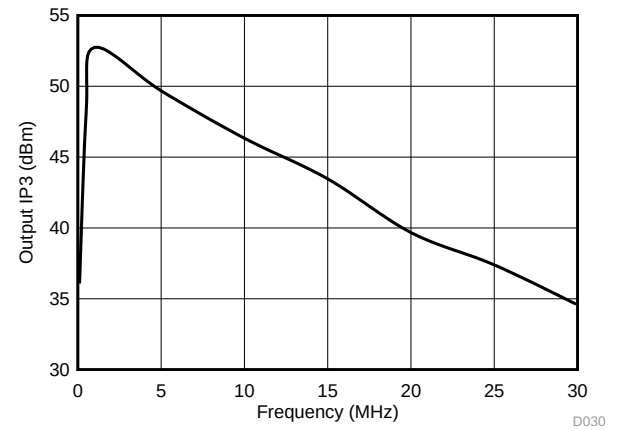
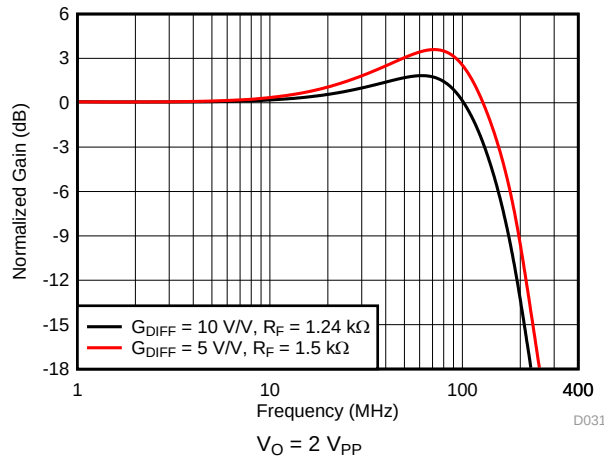


Figure 30. Two-Tone, Third-Order Intermodulation Intercept

6.10 Typical Characteristics: V_S = ±12 V (Low Bias)

at T_A = 25°C, G_{DIFF} = 10 V/V, G_{CM} = 1 V/V, R_{ADJ} = 0 Ω, R_F = 1.24 kΩ, and R_L = 100 Ω (unless otherwise noted)



V_O = 2 V_{PP}

Figure 31. Small-Signal Frequency Response

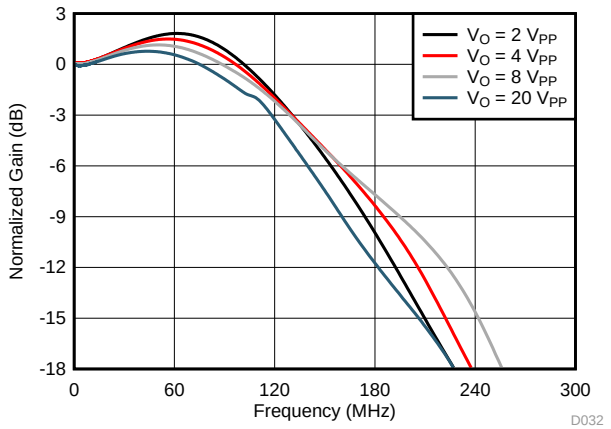


Figure 32. Large-Signal Frequency Response

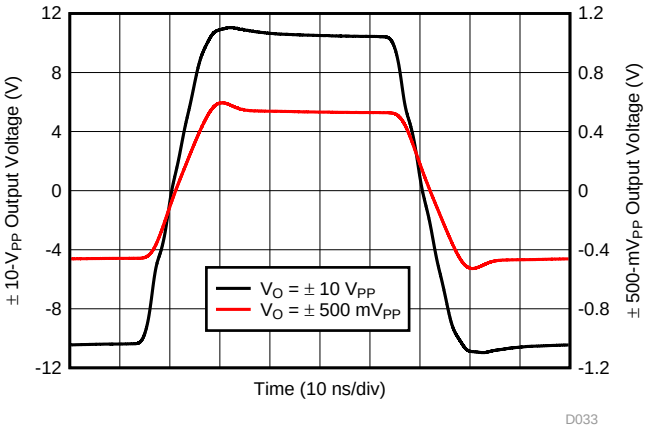


Figure 33. Pulse Response

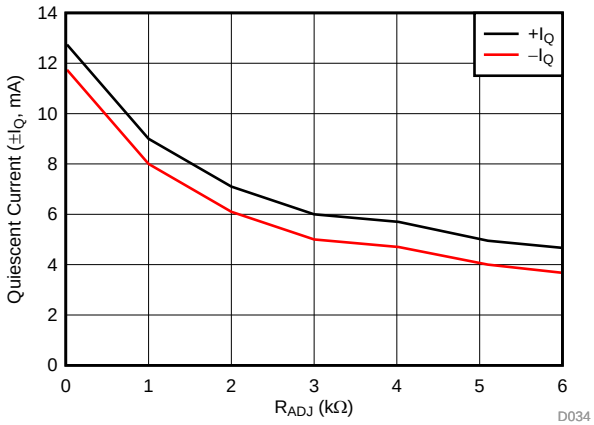


Figure 34. Supply Current for Low Bias Setting vs R_{ADJ}

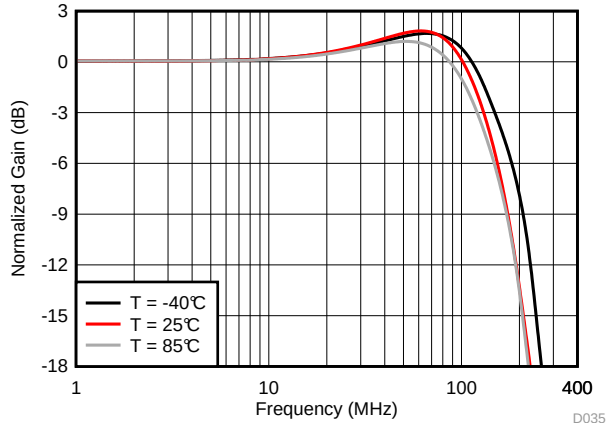
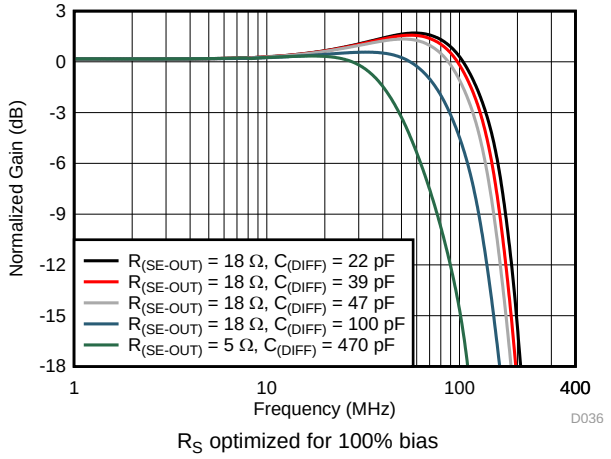


Figure 35. Frequency Response Across Temperature

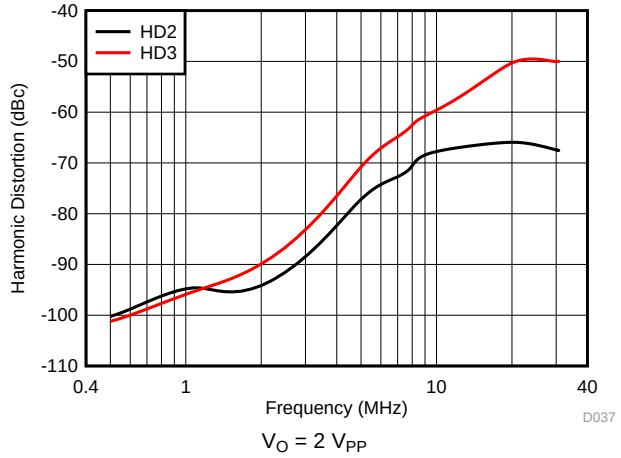


R_S optimized for 100% bias

Figure 36. Frequency Response Across Capacitive Load

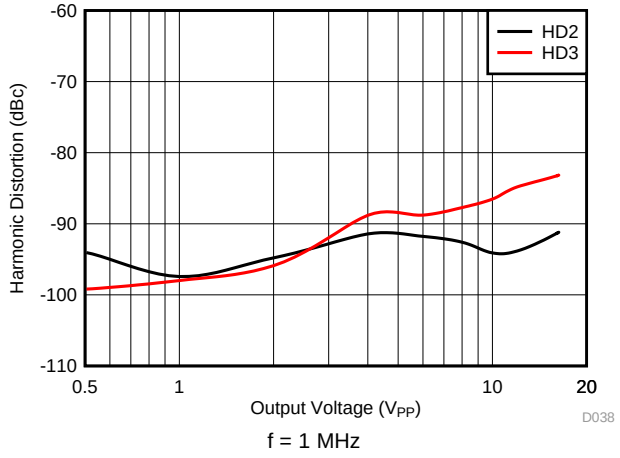
Typical Characteristics: V_S = ±12 V (Low Bias) (continued)

at T_A = 25°C, G_{DIFF} = 10 V/V, G_{CM} = 1 V/V, R_{ADJ} = 0 Ω, R_F = 1.24 kΩ, and R_L = 100 Ω (unless otherwise noted)



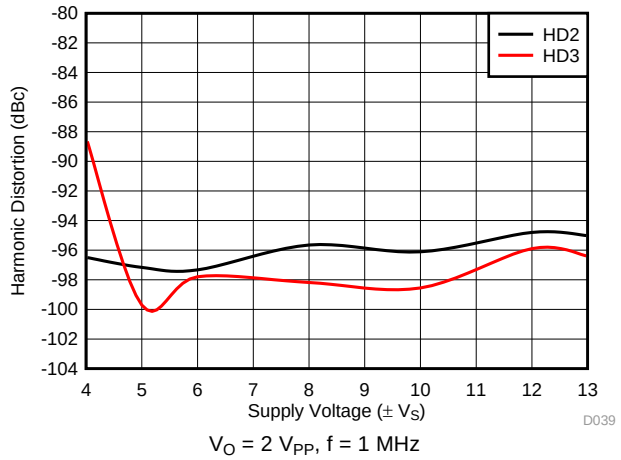
V_O = 2 V_{PP}

Figure 37. Harmonic Distortion vs Frequency



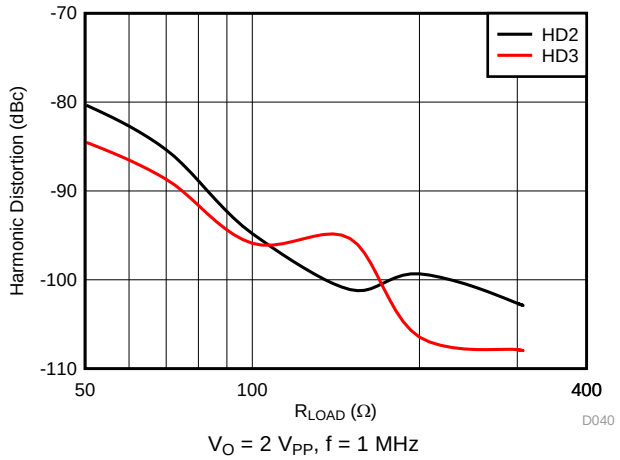
f = 1 MHz

Figure 38. Harmonic Distortion vs Output Voltage



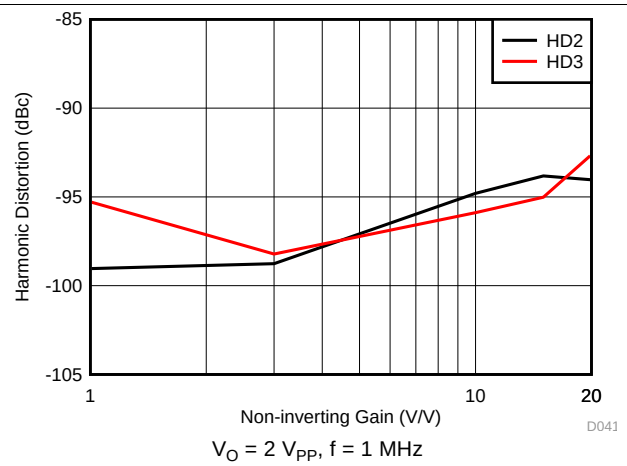
V_O = 2 V_{PP}, f = 1 MHz

Figure 39. Harmonic Distortion vs Supply Voltage



V_O = 2 V_{PP}, f = 1 MHz

Figure 40. Harmonic Distortion vs Load Resistance



V_O = 2 V_{PP}, f = 1 MHz

Figure 41. Harmonic Distortion vs Noninverting Gain

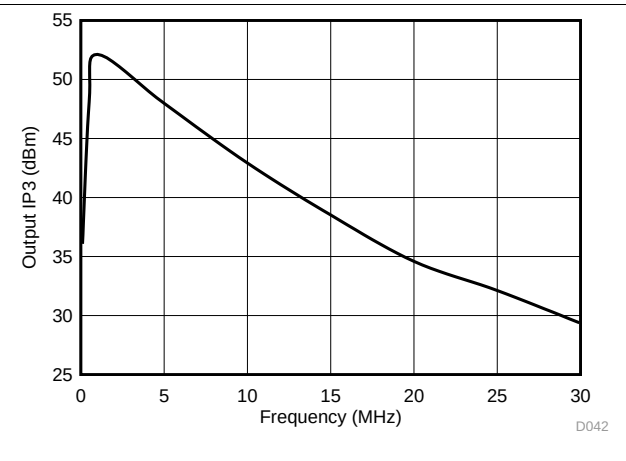


Figure 42. Two-Tone, Third-Order Intermodulation Intercept

6.11 Typical Characteristics: V_S = ±6 V (Full Bias)

at T_A = 25°C, G_{DIFF} = 5 V/V, G_{CM} = 1 V/V, R_{ADJ} = 0 Ω, R_F = 1.82 kΩ, and R_L = 100 Ω (unless otherwise noted)

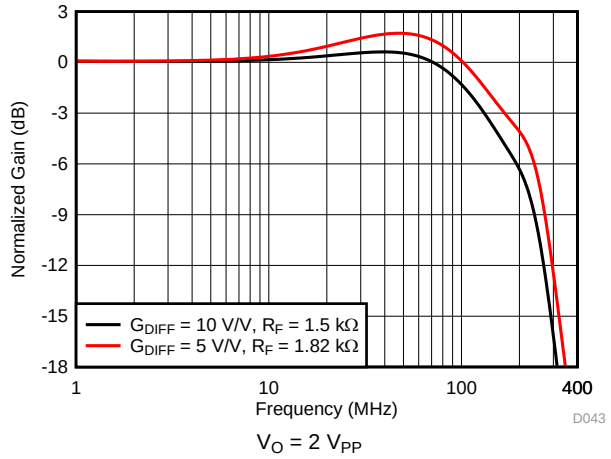


Figure 43. Small-Signal Frequency Response

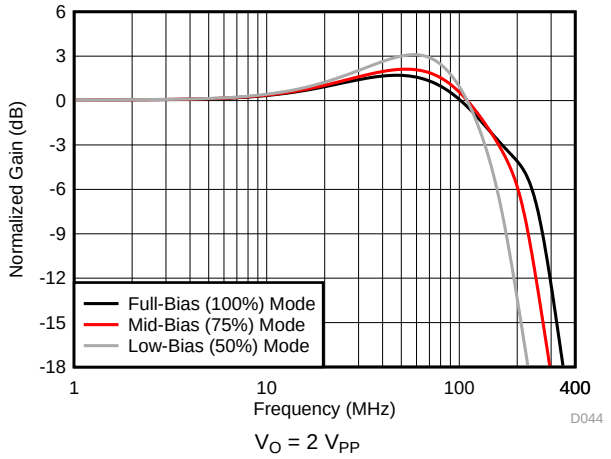


Figure 44. Small-Signal Frequency Response vs Bias

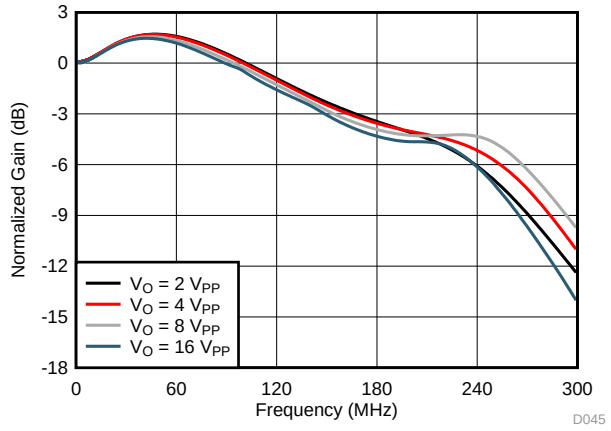


Figure 45. Large-Signal Frequency Response

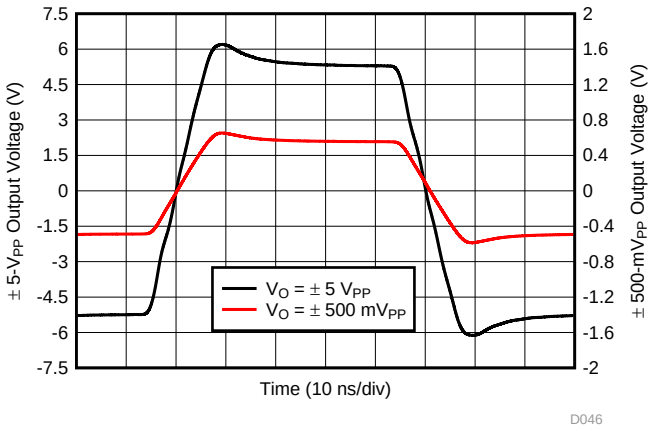


Figure 46. Pulse Response

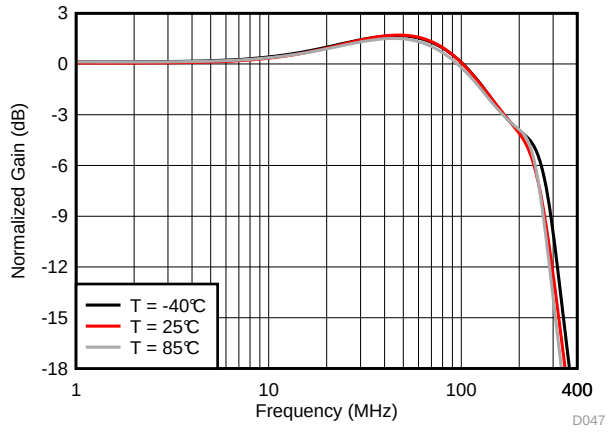


Figure 47. Frequency Response Across Temperature

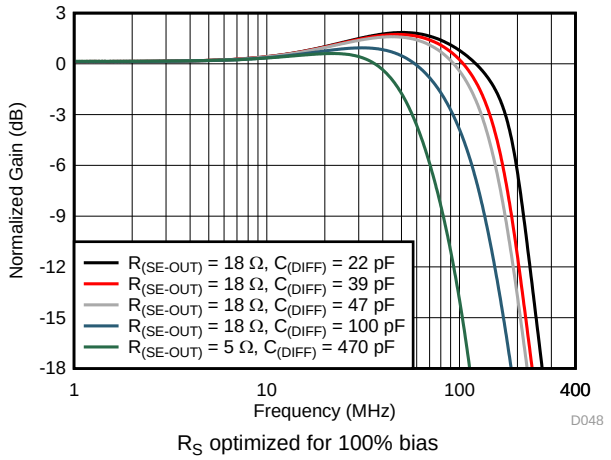
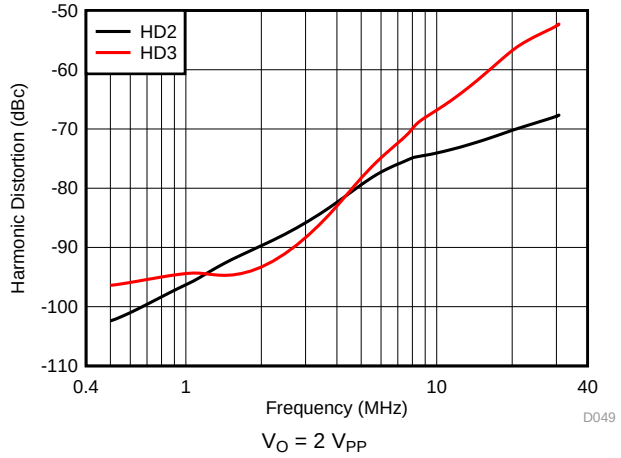


Figure 48. Frequency Response Across Capacitive Load

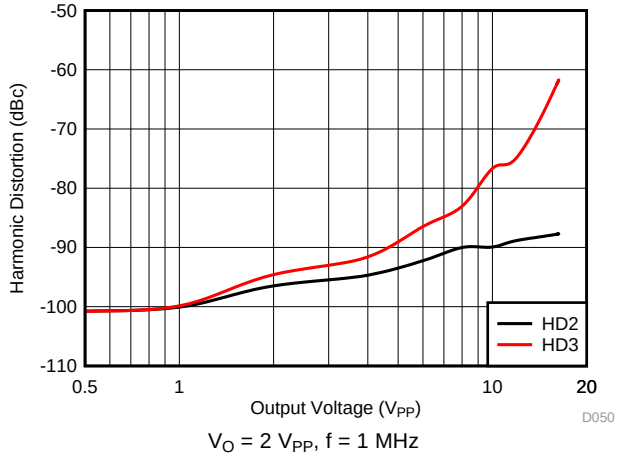
Typical Characteristics: V_S = ±6 V (Full Bias) (continued)

at T_A = 25°C, G_{DIFF} = 5 V/V, G_{CM} = 1 V/V, R_{ADJ} = 0 Ω, R_F = 1.82 kΩ, and R_L = 100 Ω (unless otherwise noted)



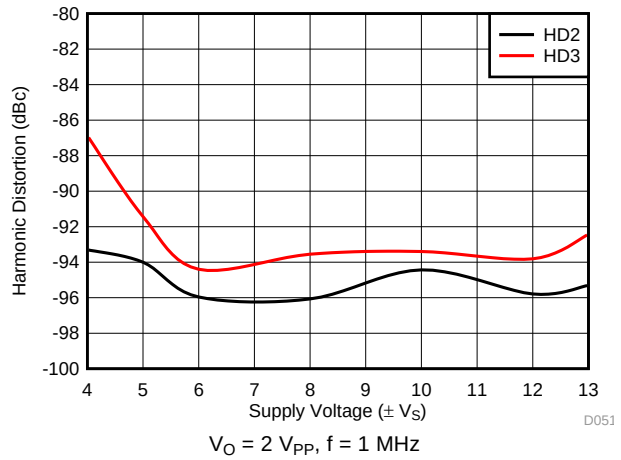
V_O = 2 V_{PP}

Figure 49. Harmonic Distortion vs Frequency



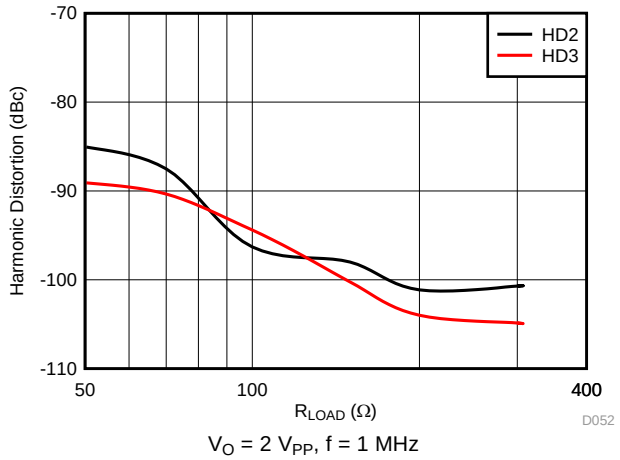
V_O = 2 V_{PP}, f = 1 MHz

Figure 50. Harmonic Distortion vs Output Voltage



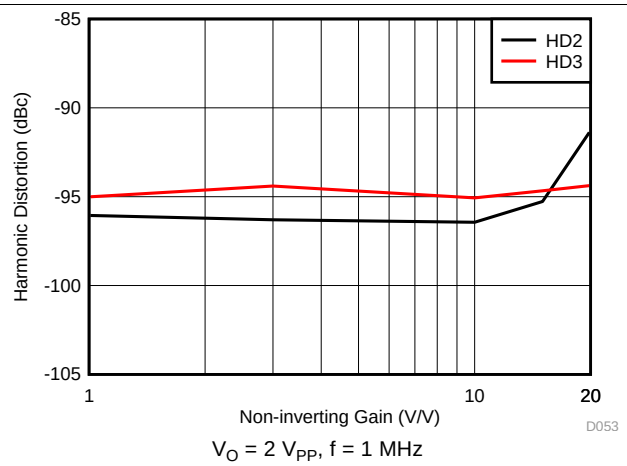
V_O = 2 V_{PP}, f = 1 MHz

Figure 51. Harmonic Distortion vs Supply Voltage



V_O = 2 V_{PP}, f = 1 MHz

Figure 52. Harmonic Distortion vs Load Resistance



V_O = 2 V_{PP}, f = 1 MHz

Figure 53. Harmonic Distortion vs Noninverting Gain

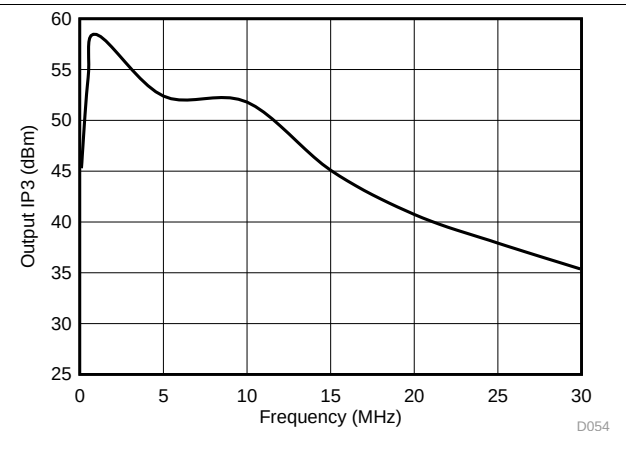


Figure 54. Two-Tone, Third-Order Intermodulation Intercept

Typical Characteristics: V_S = ±6 V (Full Bias) (continued)

at T_A = 25°C, G_{DIFF} = 5 V/V, G_{CM} = 1 V/V, R_{ADJ} = 0 Ω, R_F = 1.82 kΩ, and R_L = 100 Ω (unless otherwise noted)

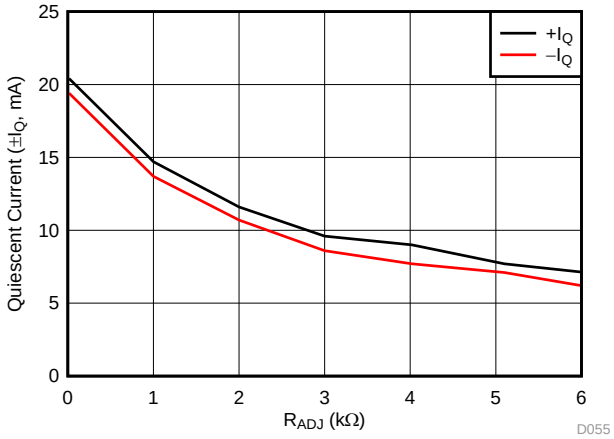


Figure 55. Quiescent Current for Full Bias Setting vs R_{ADJ}

6.12 Typical Characteristics: V_S = ±6 V (Mid Bias)

at T_A = 25°C, G_{DIFF} = 5 V/V, G_{CM} = 1 V/V, R_{ADJ} = 0 Ω, R_F = 1.82 kΩ, and R_L = 100 Ω (unless otherwise noted)

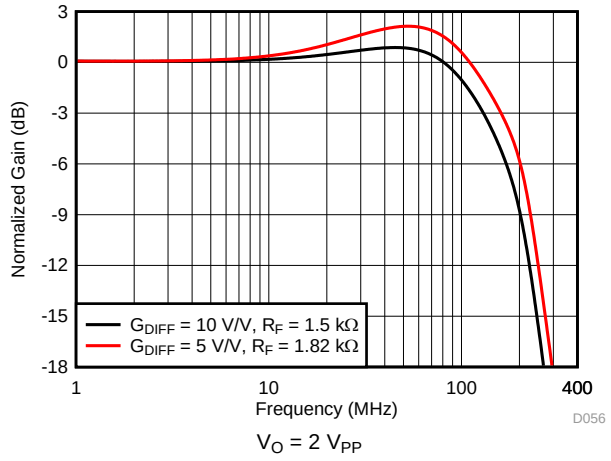


Figure 56. Small-Signal Frequency Response

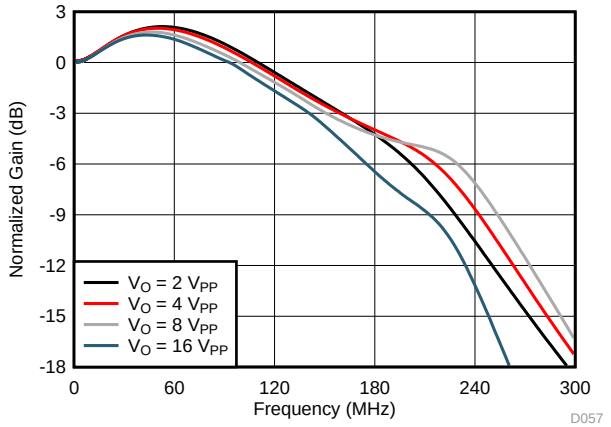


Figure 57. Large-Signal Frequency Response

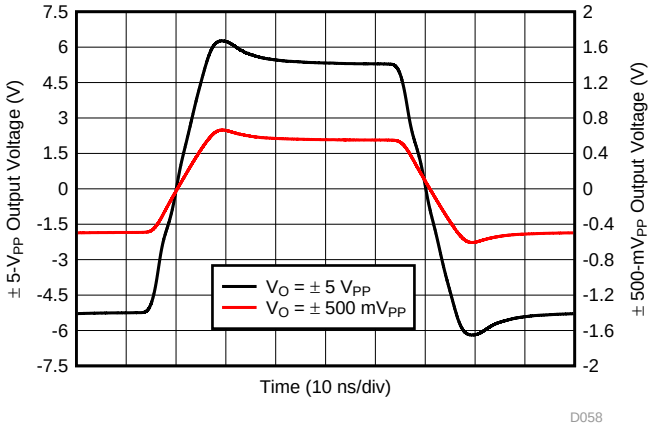


Figure 58. Pulse Response

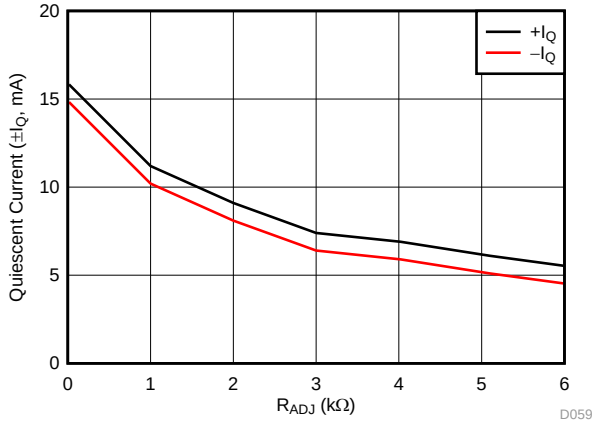


Figure 59. Quiescent Current for Mid Bias Setting vs R_{ADJ}

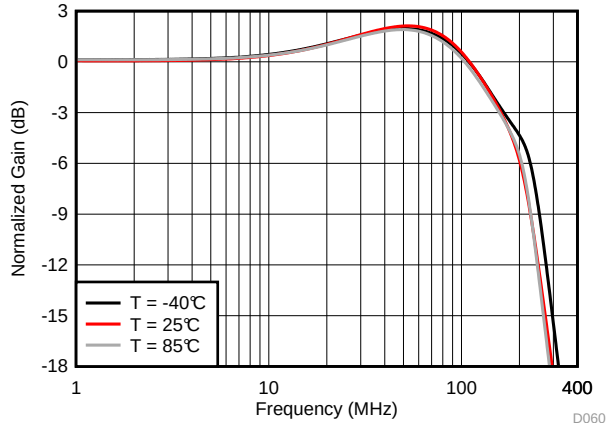


Figure 60. Frequency Response Across Temperature

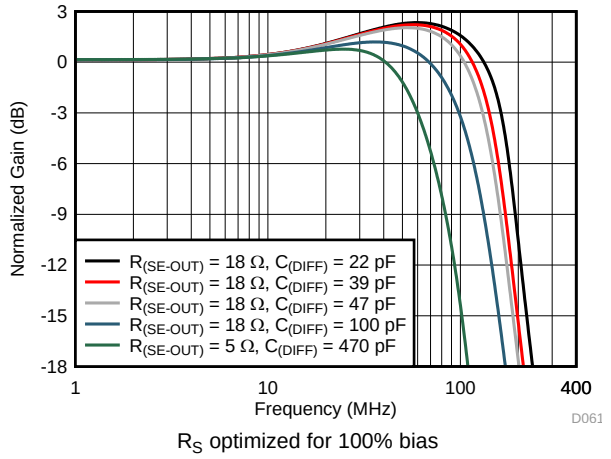
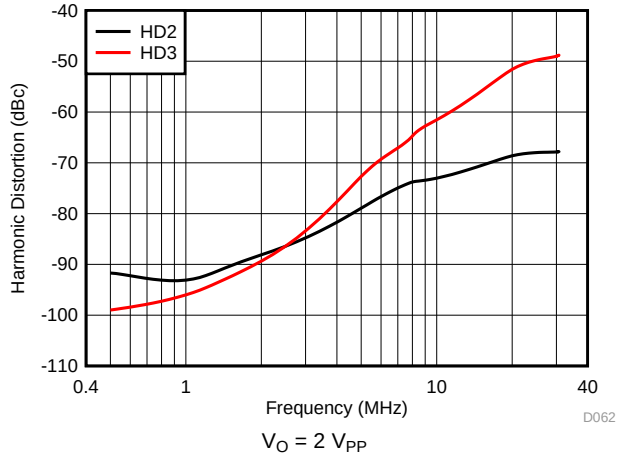


Figure 61. Frequency Response Across Capacitive Load

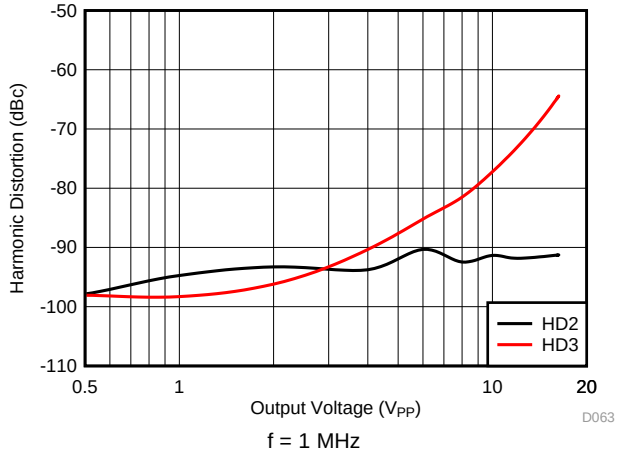
Typical Characteristics: V_S = ±6 V (Mid Bias) (continued)

at T_A = 25°C, G_{DIFF} = 5 V/V, G_{CM} = 1 V/V, R_{ADJ} = 0 Ω, R_F = 1.82 kΩ, and R_L = 100 Ω (unless otherwise noted)



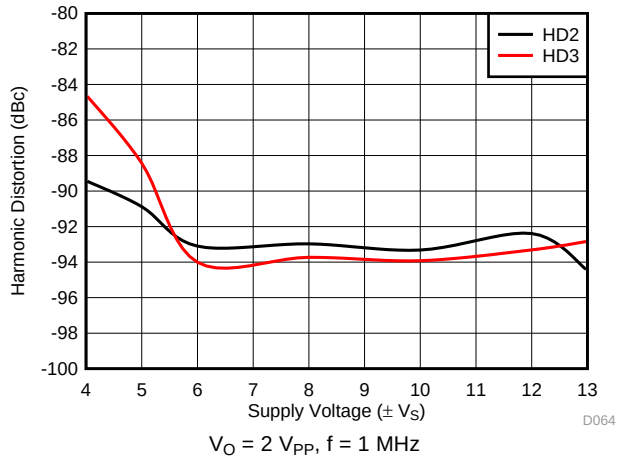
V_O = 2 V_{PP}

Figure 62. Harmonic Distortion vs Frequency



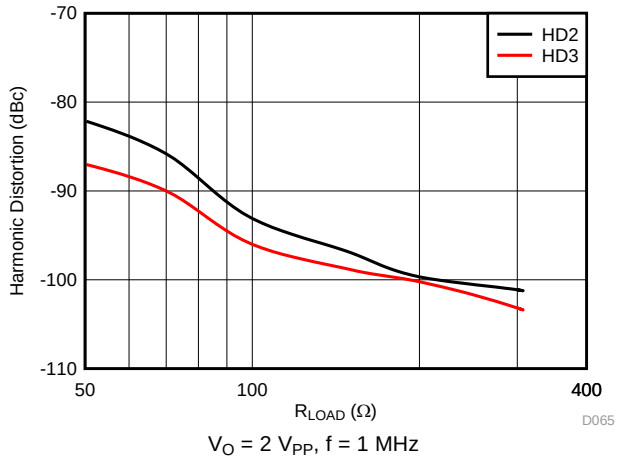
f = 1 MHz

Figure 63. Harmonic Distortion vs Output Voltage



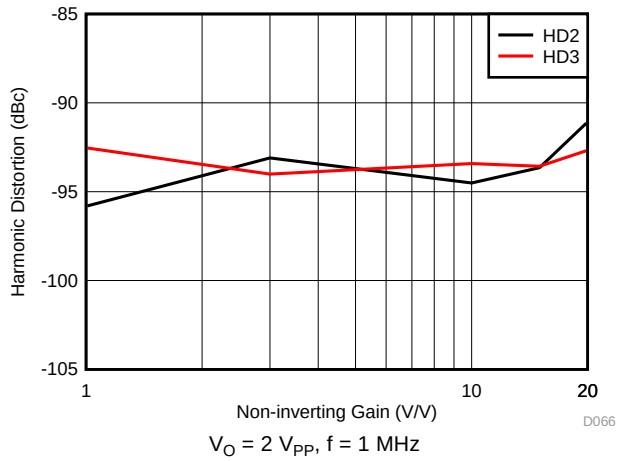
V_O = 2 V_{PP}, f = 1 MHz

Figure 64. Harmonic Distortion vs Supply Voltage



V_O = 2 V_{PP}, f = 1 MHz

Figure 65. Harmonic Distortion vs Load Resistance



V_O = 2 V_{PP}, f = 1 MHz

Figure 66. Harmonic Distortion vs Noninverting Gain

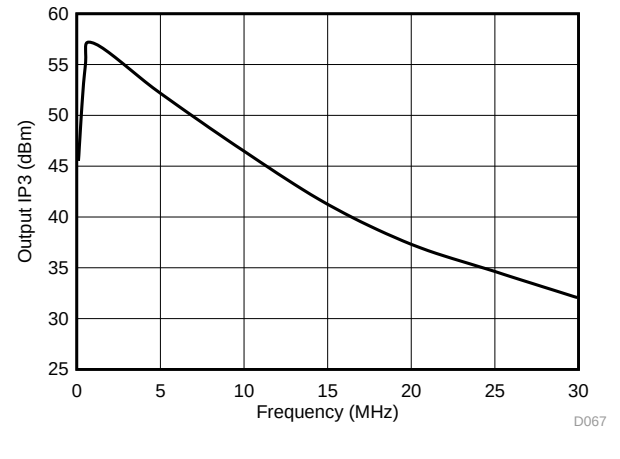


Figure 67. Two-Tone, Third-Order Intermodulation Intercept

6.13 Typical Characteristics: V_S = ±6 V (Low Bias)

at T_A = 25°C, G_{DIFF} = 5 V/V, G_{CM} = 1 V/V, R_{ADJ} = 0 Ω, R_F = 1.82 kΩ, and R_L = 100 Ω (unless otherwise noted)

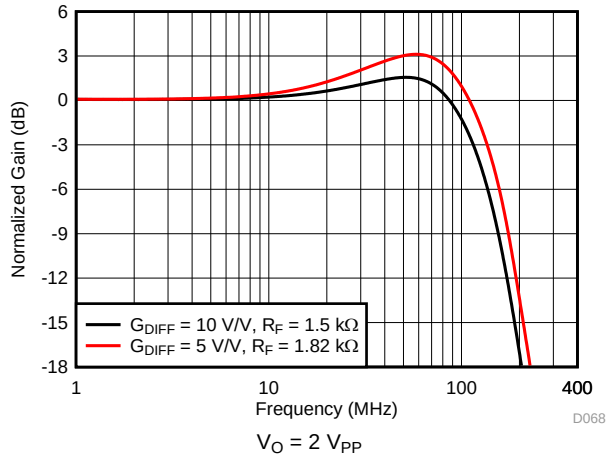


Figure 68. Small-Signal Frequency Response

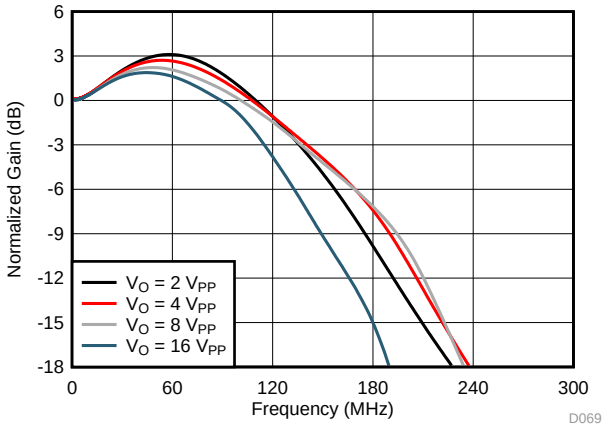


Figure 69. Large-Signal Frequency Response

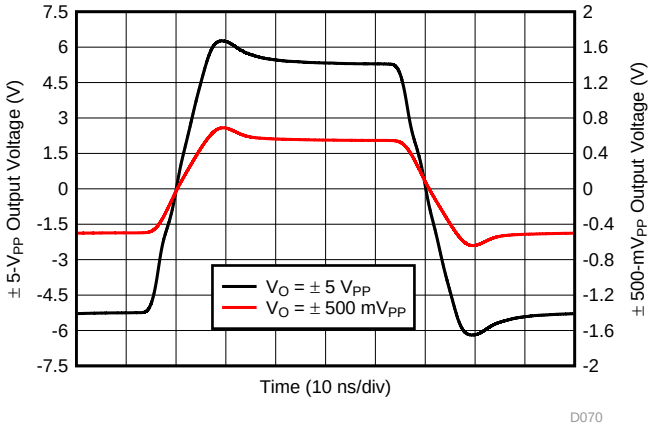


Figure 70. Pulse Response

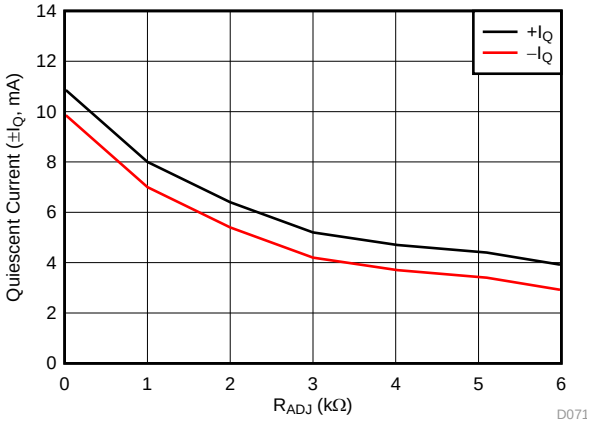


Figure 71. Quiescent Current for Low Bias Setting vs R_{ADJ}

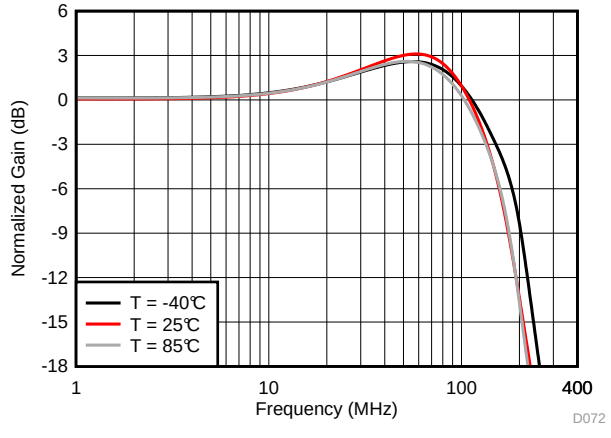


Figure 72. Frequency Response Across Temperature

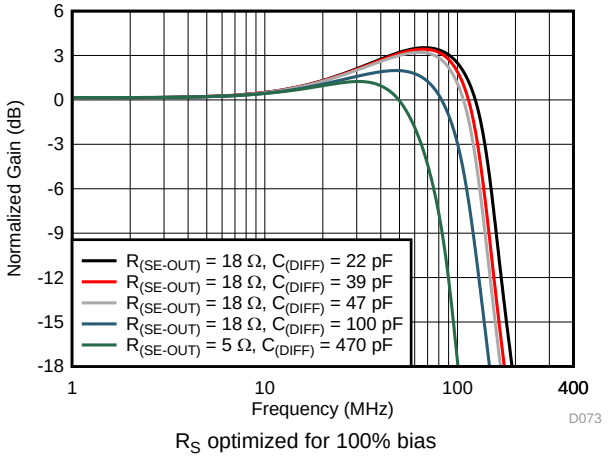
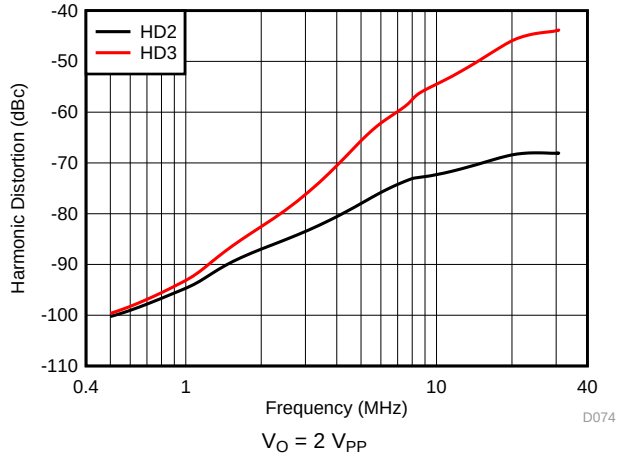


Figure 73. Frequency Response Across Capacitive Load

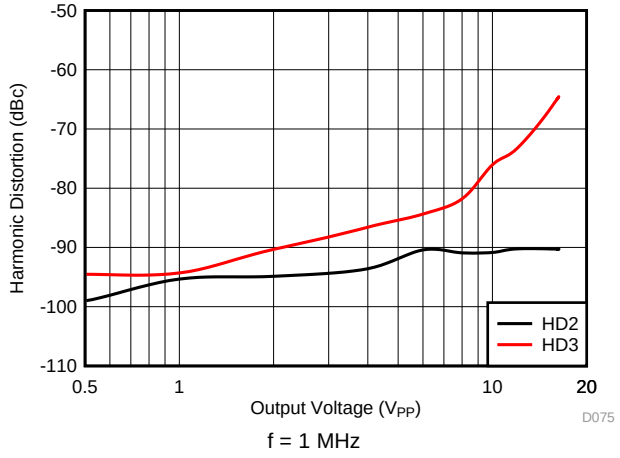
Typical Characteristics: V_S = ±6 V (Low Bias) (continued)

at T_A = 25°C, G_{DIFF} = 5 V/V, G_{CM} = 1 V/V, R_{ADJ} = 0 Ω, R_F = 1.82 kΩ, and R_L = 100 Ω (unless otherwise noted)



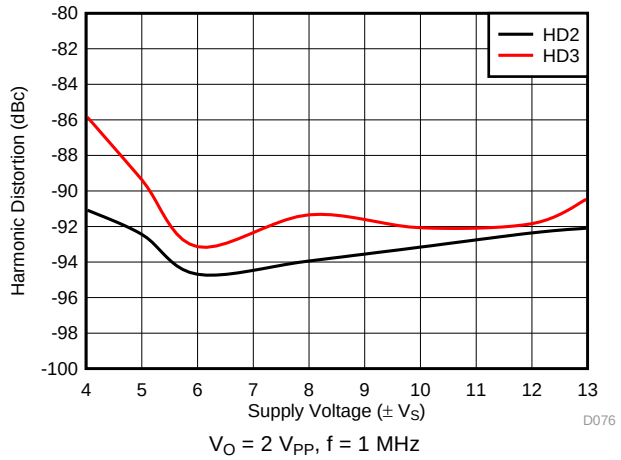
V_O = 2 V_{PP}

Figure 74. Harmonic Distortion vs Frequency



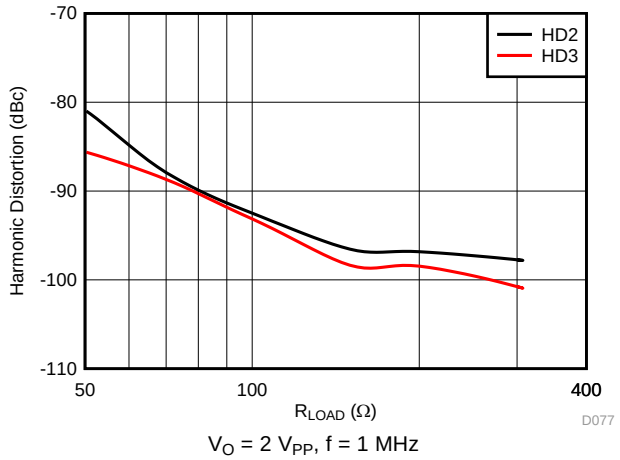
f = 1 MHz

Figure 75. Harmonic Distortion vs Output Voltage



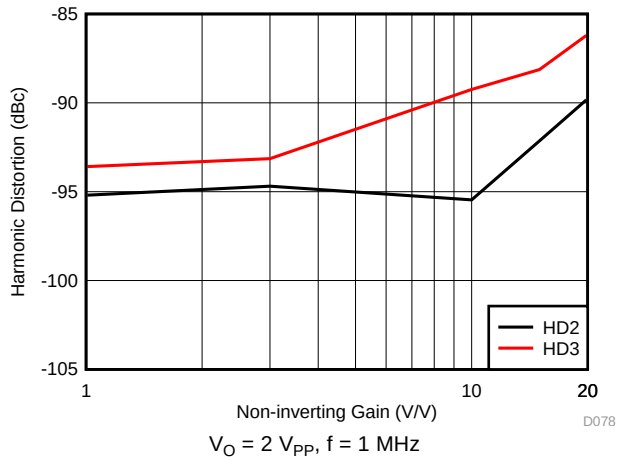
V_O = 2 V_{PP}, f = 1 MHz

Figure 76. Harmonic Distortion vs Supply Voltage



V_O = 2 V_{PP}, f = 1 MHz

Figure 77. Harmonic Distortion vs Load Resistance



V_O = 2 V_{PP}, f = 1 MHz

Figure 78. Harmonic Distortion vs Noninverting Gain

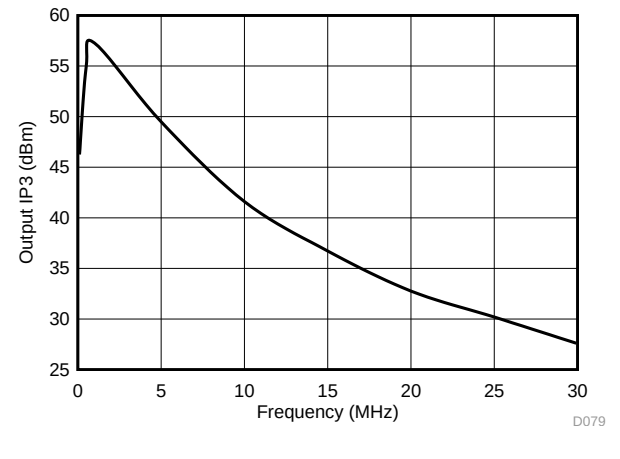


Figure 79. Two-Tone, Third-Order Intermodulation Intercept

7 Detailed Description

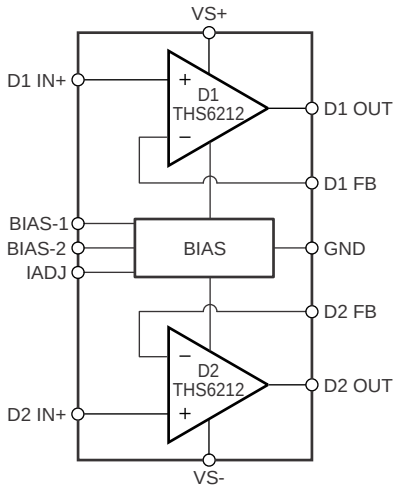
7.1 Overview

The THS6212 is a differential line-driver amplifier with a current-feedback architecture. The device is targeted for use in line-driver applications (such as wide-band power-line communications) and is fast enough to support transmissions of 14.5-dBm line power up to 30 MHz.

The THS6212 is designed as a single-channel solution that can be a drop-in replacement for dual-channel footprint packages. The package pinout is compatible with the pinout of the THS6214 dual, differential line driver, and provides an alternative for systems that only require a single-channel device.

The architecture of the THS6212 is designed to provide maximum flexibility with multiple bias settings that are selectable based on application performance requirements, and also provides an external current pin (IADJ) to further adjust the bias current to the device. The wide output swing (43.2 V_{PP}) and high current drive (416 mA) of the THS6212 make the device ideally suited for high-power, line-driving applications.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Output Current and Voltage

The THS6212 provides output voltage and current capabilities that are unsurpassed in a low-cost, monolithic op amp. Under no-load conditions at 25°C, the output voltage typically swings closer than 1.1 V to either supply rail; tested at 25°C, the swing limit is within 1.4 V of either rail into a 100-Ω differential load. Into a 25-Ω load (the minimum tested load), the amplifier delivers more than ±408-mA continuous and greater than ±1-A peak output current.

These commonly occurring specifications, though familiar in the industry, only consider voltage and current limits separately. In many applications, the voltage times current (or V-I product) is more relevant to circuit operation; see the *Output Voltage and Current Limitations* plot (Figure 13) in the *Typical Characteristics* section. The X- and Y-axes of this graph show the zero-voltage output current limit and the zero-current output voltage limit, respectively. The four quadrants give a more detailed view of the THS6212 output drive capabilities, noting that the graph is bounded by a safe operating area of a 1-W maximum internal power dissipation. Superimposing resistor load lines onto the plot illustrates that the THS6212 can drive ±10.9 V into 100 Ω or ±10.5 V into 50 Ω without exceeding the output capabilities or the 1-W dissipation limit. A 100-Ω load line (the standard test circuit load) illustrates the full ±12-V output swing capability, as provided in the *Electrical Characteristics* tables. The minimum specified output voltage and current over temperature are set by worst-case simulations at the cold temperature extreme. Only at cold startup do the output current and voltage decrease to the numbers given in the *Electrical Characteristics* tables. When the output transistors deliver power, the junction temperature increases, decreasing the V_{BE}s (increasing the available output voltage swing), and increasing the current gains (increasing the available output current). In steady-state operation, the available output voltage and current are

Feature Description (continued)

always greater than that shown in the overtemperature specifications because the output stage junction temperatures are higher than the minimum specified operating ambient temperature. To maintain maximum output stage linearity, no output short-circuit protection is provided. This absence of short-circuit protection is normally not a problem because most applications include a series-matching resistor at the output that limits the internal power dissipation if the output side of this resistor is shorted to ground. However, shorting the output pin directly to the adjacent positive power-supply pin (24-pin package), in most cases destroys the amplifier. If additional short-circuit protection is required, a small series resistor can be included in the supply lines. Under heavy output loads, this additional resistor reduces the available output voltage swing. A 5-Ω series resistor in each power-supply lead limits the internal power dissipation to less than 1 W for an output short-circuit, and decreases the available output voltage swing by only 0.5 V for up to 100-mA desired load currents. Always place the 0.1-µF power-supply decoupling capacitors after these supply current limiting resistors, directly on the supply pins.

7.3.2 Driving Capacitive Loads

One of the most demanding and yet very common load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an ADC—including additional external capacitance that can be recommended to improve the ADC linearity. A high-speed, high open-loop gain amplifier such as the THS6212 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the amplifier open-loop output resistance is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin. One external solution to this problem is described in this section.

When the primary considerations are frequency response flatness, pulse response fidelity, and distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load. This series resistor does not eliminate the pole from the loop response, but shifts the pole and adds a zero at a higher frequency. The additional zero functions to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability. The *Typical Characteristics* sections describe the recommended R_S versus capacitive load (see Figure 5, Figure 23, Figure 35, Figure 47, Figure 60, and Figure 72) and the resulting frequency response at the load. Parasitic capacitive loads greater than 2 pF can begin to degrade device performance. Long printed-circuit board (PCB) traces, unmatched cables, and connections to multiple devices can easily cause this value to be exceeded. Always consider this effect carefully, and add the recommended series resistor as close as possible to the THS6212 output pin (see the *Layout Guidelines* section).

7.3.3 Distortion Performance

The THS6212 provides good distortion performance into a 100-Ω load on ±12-V supplies. Relative to alternative solutions, the amplifier provides exceptional performance into lighter loads and operation on a dual ±6-V supply. Generally, until the fundamental signal reaches very high frequency or power levels, the second harmonic dominates the distortion with a negligible third-harmonic component. Focusing then on the second harmonic, increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network—in the noninverting configuration (see Figure 81), this value is the sum of $R_F + R_G$, whereas in the inverting configuration this value is just R_F. Providing an additional supply decoupling capacitor (0.01 µF) between the supply pins (for bipolar operation) also improves the second-order distortion slightly (from 3 dB to 6 dB).

In most op amps, increasing the output voltage swing directly increases harmonic distortion. The *Typical Characteristics* sections illustrate the second harmonic increasing at a little less than the expected 2x rate, whereas the third harmonic increases at a little less than the expected 3x rate. Where the test power doubles, the difference between the fundamental power and the second harmonic decreases less than the expected 6 dB, whereas the difference between the fundamental power and the third harmonic decreases by less than the expected 12 dB. This difference also appears in the two-tone, third-order intermodulation (IM3) spurious response curves. The third-order spurious levels are extremely low at low-output power levels. The output stage continues to hold the third-order spurious levels low even when the fundamental power reaches very high levels.

Feature Description (continued)

7.3.4 Differential Noise Performance

The THS6212 is designed to be used as a differential driver in high-performance applications. Therefore, analyzing the noise in such a configuration is important. Figure 80 shows the op amp noise model for the differential configuration.

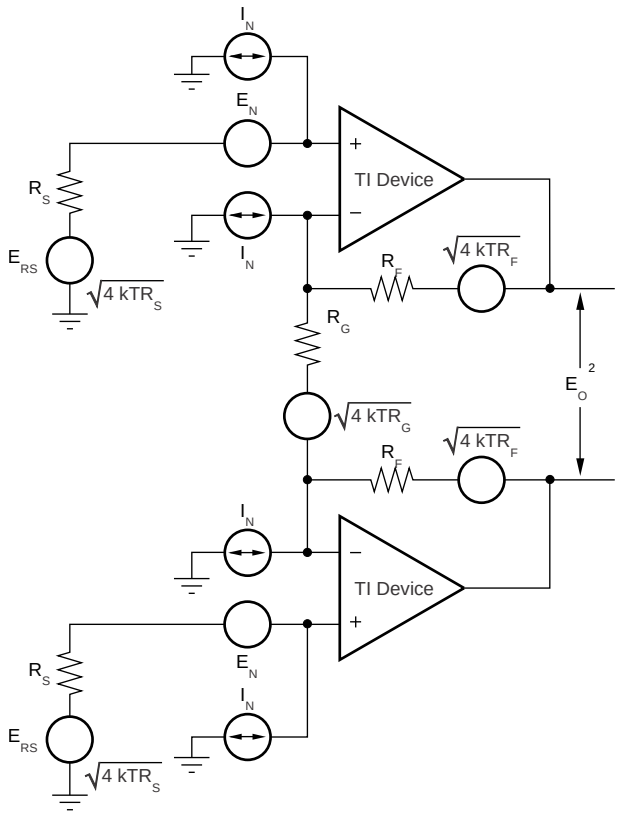


Figure 80. Differential Op Amp Noise Analysis Model

As a reminder, the differential gain is expressed in Equation 1:

$$G_D = 1 + \frac{2 \times R_F}{R_G} \tag{1}$$

The output noise can be expressed as shown in Equation 2:

$$E_O = \sqrt{2 \times G_D^2 \times \left[e_N^2 + (i_N \times R_S)^2 + 4\ kTR_S\right] + 2(i_l R_F)^2 + 2(4\ kTR_F G_D)} \tag{2}$$

Dividing this expression by the differential noise gain [$G_D = (1 + 2R_F / R_G)$] gives the equivalent input-referred spot noise voltage at the noninverting input, as shown in Equation 3.

$$E_O = \sqrt{2 \times \left[e_N^2 + (i_N \times R_S)^2 + 4\ kTR_S\right] + 2\left[\frac{i_l R_F}{G_D}\right]^2 + 2\left[\frac{4\ kTR_F}{G_D}\right]} \tag{3}$$

Evaluating these equations for the THS6212 circuit and component values of Figure 84 gives a total output spot noise voltage of 38.9 nV/√Hz and a total equivalent input spot noise voltage of 7 nV/√Hz.

In order to minimize the output noise as a result of the noninverting input bias current noise, keeping the noninverting source impedance as low as possible is recommended.

Feature Description (continued)

7.3.5 DC Accuracy and Offset Control

A current-feedback op amp such as the THS6212 provides exceptional bandwidth in high gains, giving fast pulse settling but only moderate dc accuracy. The *Electrical Characteristics* tables describe an input offset voltage that is comparable to high-speed, voltage-feedback amplifiers; however, the two input bias currents are somewhat higher and are unmatched. Although bias current cancellation techniques are very effective with most voltage-feedback op amps, these techniques do not generally reduce the output dc offset for wideband current-feedback op amps. Because the two input bias currents are unrelated in both magnitude and polarity, matching the input source impedance to reduce error contribution to the output is ineffective. Evaluating the configuration of Figure 81, using a worst-case condition at 25°C input offset voltage and the two input bias currents, gives a worst-case output offset range equal to Equation 4:

$$V_{OFF} = \pm\left(NG \times V_{OS(MAX)}\right) + \left(I_{BN} \times \frac{R_S}{2} \times NG\right) \pm \left(I_{BI} \times R_F\right)$$

$$= \pm\left(10 \times 5\ mV\right) + \left(3.5\ \mu A \times 25\ \Omega \times 10\right) \pm \left(1.24\ k\Omega \times 45\ \mu A\right)$$

$$= \pm 50\ mV + 0.875\ mV \pm 55.5\ mV$$

$$V_{OFF} = -104.92\ mV \text{ to } 106.67\ mV \quad (4)$$

where

- NG = noninverting signal gain

7.4 Device Functional Modes

The THS6212 has four different functional modes set by the BIAS-1 and BIAS-2 pins. Table 1 shows the truth table for the device mode pin configuration and the associated description of each mode.

Table 1. BIAS-1 and BIAS-2 Logic Table

BIAS-1	BIAS-2	FUNCTION	DESCRIPTION
0	0	Full-bias mode (100%)	Amplifiers on with lowest distortion possible (default state)
1	0	Mid-bias mode (75%)	Amplifiers on with power savings and a reduction in distortion performance
0	1	Low-bias mode (50%)	Amplifiers on with enhanced power savings and a reduction of overall performance
1	1	Shutdown mode	Amplifiers off and output has high impedance

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The THS6212 is typically used to drive high output power applications with various load conditions. In the *Typical Applications* section, the amplifier is presented in a general-purpose, wideband, current-feedback configuration, and a more specific 100-Ω twisted pair cable line driver. However, the amplifier is also applicable for many different general-purpose and specific cable line-driving scenarios beyond what is shown in the *Typical Applications* section.

8.2 Typical Applications

8.2.1 Wideband Current-Feedback Operation

The THS6212 provides the exceptional ac performance of a wideband current-feedback op amp with a highly linear, high-power output stage. Requiring only 23 mA of quiescent current, the THS6212 swings to within 1.9 V of either supply rail on a 100-Ω load and delivers in excess of 416 mA at room temperature. This low-output headroom requirement, along with biasing that is independent of the supply voltage, provides a remarkable ±6-V supply operation. The THS6212 delivers greater than 140-MHz bandwidth driving a 2-V_{PP} output into 100 Ω on a ±6-V supply. Previous boosted output stage amplifiers typically suffer from very poor crossover distortion when the output current goes through zero. The THS6212 achieves a comparable power gain with improved linearity. The primary advantage of a current-feedback op amp over a voltage-feedback op amp is that ac performance (bandwidth and distortion) is relatively independent of signal gain. Figure 81 shows the dc-coupled, gain of 10 V/V, dual power-supply circuit configuration used as the basis of the ±12-V *Electrical Characteristics* tables and *Typical Characteristics* sections.

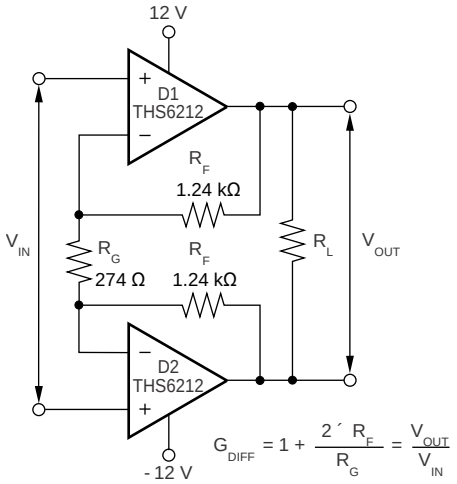


Figure 81. Noninverting Differential I/O Amplifier

8.2.1.1 Design Requirements

The main design requirements for wideband current-feedback operation are to choose power supplies that satisfy common-mode requirements at the input and output of the device, and also to use a feedback resistor value that allows for the proper bandwidth when maintaining stability. These requirements and the proper solutions are described in the *Detailed Design Procedure* section. Using transformers and split power supplies can be required for certain applications.

Typical Applications (continued)

8.2.1.2 Detailed Design Procedure

For ease of test purposes in this design, the THS6212 input impedance is set to 50 Ω with a resistor to ground and the output impedance is set to 50 Ω with a series output resistor. Voltage swings reported in the *Electrical Characteristics* tables are taken directly at the input and output pins, whereas load powers (dBm) are defined at a matched 50-Ω load. For the circuit of Figure 81, the total effective load is 100 Ω || 1.24 kΩ || 1.24 kΩ = 86.1 Ω. This approach allows a source termination impedance to be set at the input that is independent of the signal gain. For instance, simple differential filters can be included in the signal path right up to the noninverting inputs with no interaction with the gain setting. The differential signal gain for the circuit of Figure 81 is given by Equation 5:

$$A_D = 1 + 2 \times \frac{R_F}{R_G} \quad (5)$$

where

- A_D = differential gain

A value of 274 Ω for the A_D = 10-V/V design is given by Figure 81. The device bandwidth is primarily controlled with the feedback resistor value because the THS6212 is a current-feedback (CFB) amplifier; the differential gain, however, can be adjusted with considerable freedom using just the R_G resistor. In fact, R_G can be reduced by a reactive network that provides a very isolated shaping to the differential frequency response.

Various combinations of single-supply or ac-coupled gain can also be delivered using the basic circuit of Figure 81. Common-mode bias voltages on the two noninverting inputs pass on to the output with a gain of 1 V/V because an equal dc voltage at each inverting node does not create current through R_G. This circuit does show a common-mode gain of 1 V/V from the input to output. The source connection must either remove this common-mode signal if undesired (using an input transformer can provide this function), or the common-mode voltage at the inputs can be used to set the output common-mode bias. If the low common-mode rejection of this circuit is a problem, the output interface can also be used to reject that common-mode signal. For instance, most modern differential input analog-to-digital converters (ADCs) reject common-mode signals very well, and a line-driver application through a transformer also attenuates the common-mode signal through to the line.

8.2.1.3 Application Curves

Figure 82 and Figure 83 show the frequency response and distortion performance of the circuit in Figure 81. The measurements are made with a load resistor (R_L) of 100 Ω, and at room temperature. Figure 82 is measured using the three different device power modes, and the distortion measurements in Figure 83 are made at an output voltage level of 2 V_{PP}.

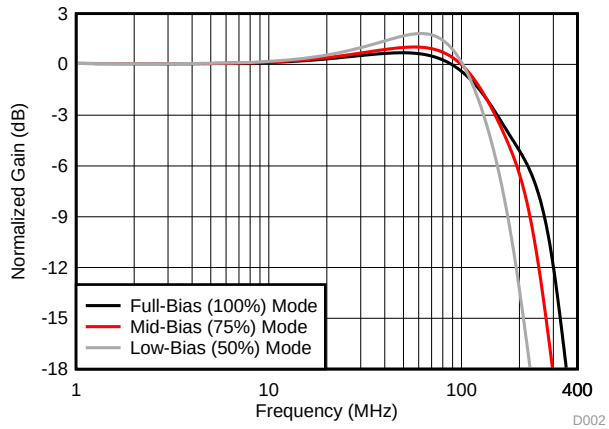


Figure 82. Frequency Response

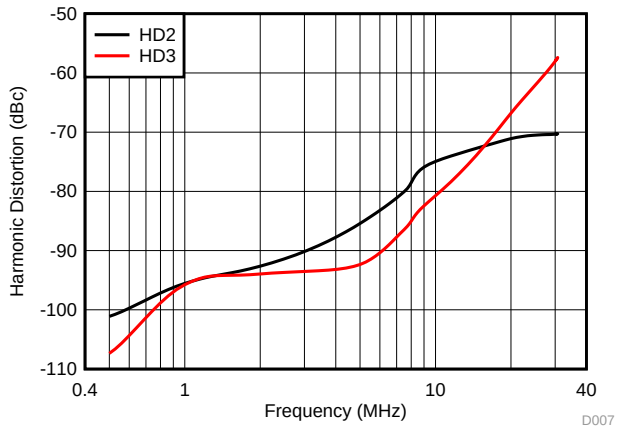


Figure 83. Harmonic Distortion

Typical Applications (continued)

8.2.2 Dual-Supply Downstream Driver

Figure 84 shows an example of a dual-supply downstream driver with a synthesized output impedance circuit. The THS6212 is configured as a differential gain stage to provide a signal drive to the primary winding of the transformer (a step-up transformer with a turns ratio of 1:n is shown in Figure 84). The main advantage of this configuration is the cancellation of all even harmonic-distortion products. Another important advantage is that each amplifier must only swing half of the total output required driving the load.

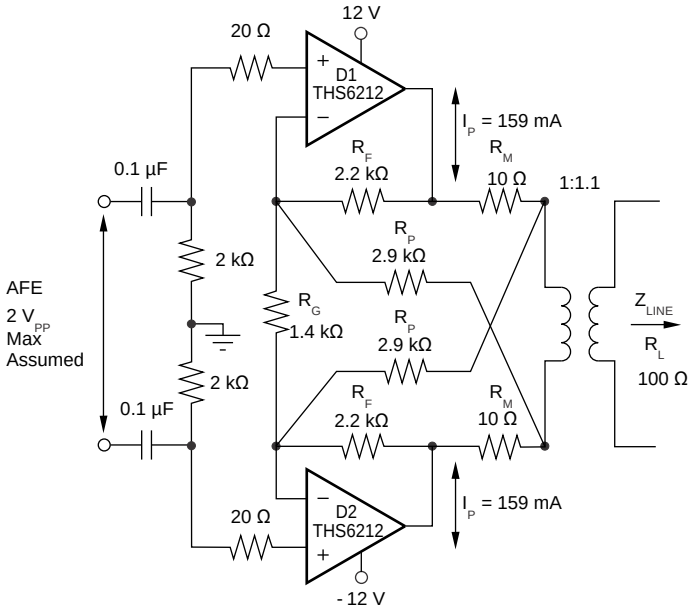


Figure 84. Dual-Supply Downstream Driver

The analog front-end (AFE) signal is ac-coupled to the driver, and the noninverting input of each amplifier is biased to the mid-supply voltage (ground in this case). In addition to providing the proper biasing to the amplifier, this approach also provides a high-pass filtering with a corner frequency that is set at 5 kHz in this example. Because the signal bandwidth starts at 26 kHz, this high-pass filter does not generate any problems and has the advantage of filtering out unwanted lower frequencies.

8.2.2.1 Design Requirements

The main design requirements for Figure 84 are to match the output impedance correctly, satisfy headroom requirements, and ensure that the circuit meets power driving requirements. These requirements are described in the *Detailed Design Procedure* section and include the required equations to properly implement the design. The design must be fully worked through before physical implementation because small changes in a single parameter can often have large effects on performance.

8.2.2.2 Detailed Design Procedure

For Figure 84, the input signal is amplified with a gain set by Equation 6:

$$G_D = 1 + \frac{2 \times R_F}{R_G} \quad (6)$$

Typical Applications (continued)

The two back-termination resistors (R_M = 10 Ω, each) added at each terminal of the transformer make the impedance of the amplifier match the impedance of the line, and also provide a means of detecting the received signal for the receiver. The value of these resistors (R_M) is a function of the line impedance and the transformer turns ratio (n), given by Equation 7:

$$R_M = \frac{Z_{LINE}}{2n^2} \tag{7}$$

8.2.2.2.1 Line Driver Headroom Requirements

The first step in a transformer-coupled, twisted-pair driver design is to compute the peak-to-peak output voltage from the target specifications. This calculation is done using Equation 8 to Equation 11:

$$P_L = 10 \times \log \frac{V_{RMS}^2}{(1\ mW) \times R_L} \tag{8}$$

where

- P_L = power at the load
- V_{RMS} = voltage at the load
- R_L = load impedance

These values produce the following:

$$V_{RMS} = \sqrt{(1\ mW) \times R_L \times 10^{\frac{P_L}{10}}} \tag{9}$$

$$V_P = \text{Crest Factor} \times V_{RMS} = CF \times V_{RMS} \tag{10}$$

where

- V_P = peak voltage at the load
- CF = crest factor

$$V_{LPP} = 2 \times CF \times V_{RMS} \tag{11}$$

where

- V_{LPP} = peak-to-peak voltage at the load

Consolidating Equation 8 to Equation 11 allows the required peak-to-peak voltage at the load to be expressed as a function of the crest factor, the load impedance, and the power at the load, as given by Equation 12:

$$V_{LPP} = 2 \times CF \times \sqrt{(1\ mW) \times R_L \times 10^{\frac{P_L}{10}}} \tag{12}$$

V_{LPP} is usually computed for a nominal line impedance and can be taken as a fixed design target.

The next step in the design is to compute the individual amplifier output voltage and currents as a function of peak-to-peak voltage on the line and transformer-turns ratio.

When this turns ratio changes, the minimum allowed supply voltage also changes. The peak current in the amplifier output is given by Equation 13:

$$\pm I_P = \frac{1}{2} \times \frac{2 \times V_{LPP}}{n} \times \frac{1}{4\ R_M} \tag{13}$$

where

- V_{PP} is as defined in Equation 12, and
- R_M is as defined in Equation 7 and Figure 85

Typical Applications (continued)

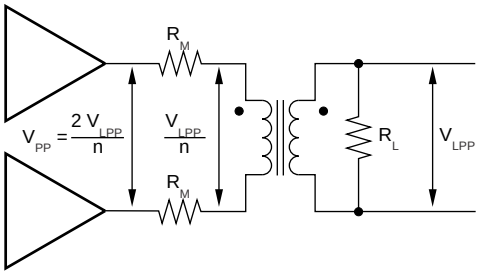


Figure 85. Driver Peak Output Voltage

With the previous information available, a supply voltage and the turns ratio desired for the transformer can now be selected, and the headroom for the THS6212 can be calculated.

The model shown in Figure 86 can be described with Equation 14 and Equation 15 as:

1. The available output swing:

$$V_{PP} = V_{CC} - (V_1 + V_2) - I_P \times (R_1 + R_2) \quad (14)$$

2. Or as the required supply voltage:

$$V_{CC} = V_{PP} + (V_1 + V_2) + I_P \times (R_1 + R_2) \quad (15)$$

The minimum supply voltage for power and load requirements is given by Equation 15.

V_1, V_2, R_1, and R_2 are given in Table 2 for the ±12-V operation.

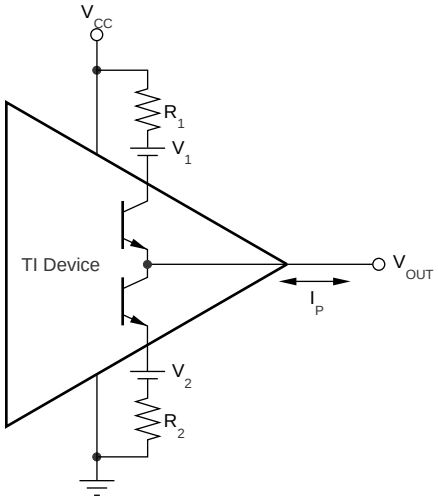


Figure 86. Line Driver Headroom Model

Table 2. Line Driver Headroom Model Values

V_S	V_1	R_1	V_2	R_2
±12 V	1 V	0.6 Ω	1 V	1.2 Ω

When using a synthetic output impedance circuit (see Figure 84), a significant drop in bandwidth occurs from the specification provided in the *Electrical Characteristics* tables. This apparent drop in bandwidth for the differential signal is a result of the apparent increase in the feedback transimpedance for each amplifier. This feedback transimpedance equation is given by Equation 16:

$$Z_{FB} = R_F \times \frac{1 + 2 \times \frac{R_S}{R_L} + \frac{R_S}{R_P}}{1 + 2 \times \frac{R_S}{R_L} + \frac{R_S}{R_P} - \frac{R_F}{R_P}} \quad (16)$$

To increase the 0.1-dB flatness to the frequency of interest, adding a serial RC in parallel with the gain resistor may be needed, as shown in Figure 87.

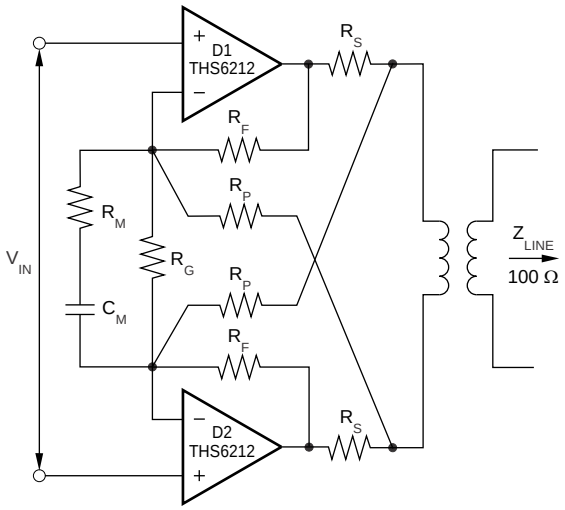


Figure 87. 0.1-dB Flatness Compensation Circuit

8.2.2.2.2 Computing Total Driver Power for Line-Driving Applications

The total internal power dissipation for the THS6212 in a line-driver application is the sum of the quiescent power and the output stage power. The THS6212 holds a relatively constant quiescent current versus supply voltage—giving a power contribution that is simply the quiescent current times the supply voltage used (the supply voltage is greater than the solution given in Equation 15). The total output stage power can be computed with reference to Figure 88.

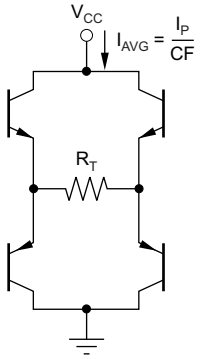


Figure 88. Output Stage Power Model

The two output stages used to drive the load of Figure 85 are shown as an H-Bridge in Figure 88. The average current drawn from the supply into this H-Bridge and load is the peak current in the load given by Equation 13 divided by the crest factor (CF) for the signal modulation. This total power from the supply is then reduced by the power in R_T, leaving the power dissipated internal to the drivers in the four output stage transistors. That power is simply the target line power used in Equation 8 plus the power lost in the matching elements (R_M). In the following examples, a perfect match is targeted giving the same power in the matching elements as in the load. The output stage power is then set by Equation 17.

$$P_{OUT} = \frac{I_P}{CF} \times V_{CC} - 2P_L \tag{17}$$

The total amplifier power is then given by Equation 18:

$$P_{TOT} = I_Q \times V_{CC} + \frac{I_P}{CF} \times V_{CC} - 2P_L \tag{18}$$

For the example given by Figure 84, the peak current is 159 mA for a signal that requires a crest factor of 5.6 with a target line power of 20.5 dBm into a 100-Ω load (115 mW).

With a typical quiescent current of 23 mA and a nominal supply voltage of ±12 V, the total internal power dissipation for the solution of Figure 84 is given by Equation 19:

$$P_{TOT} = 23\ mA\ (24\ V) + \frac{159\ mA}{5.6}\ (24\ V) - 2(115\ mW) = 1003\ mW \tag{19}$$

8.3 Do's and Don'ts

8.3.1 Do

- Include a thermal design at the beginning of the project.
- Use well-terminated transmission lines for all signals.
- Use solid metal layers for the power supplies.
- Keep signal lines as straight as possible.
- Use split supplies where required.

8.3.2 Don't

- Use a lower supply voltage than necessary.
- Use thin metal traces to supply power.
- Forget about the common-mode response of filters and transmission lines.

9 Power Supply Recommendations

The THS6212 is designed to operate optimally using split power supplies. The device has a very wide supply range of ±5 V to ±14 V to accommodate many different application scenarios. Choose power-supply voltages that allow for adequate swing on both the inputs and outputs of the amplifier to prevent affecting device performance. The ground pin provides the ground reference for the control pins and must be within $V_{S–}$ to (V_{S+} – 5 V) for proper operation.

10 Layout

10.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier such as the THS6212 requires careful attention to board layout parasitic and external component types. Recommendations that optimize performance include:

a. Minimize parasitic capacitance to any ac ground for all signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability; on the noninverting input, this capacitance can react with the source impedance to cause unintentional band limiting. To reduce unwanted capacitance, a window around the signal I/O pins must be opened in all ground and power planes around these pins. Otherwise, ground and power planes must be unbroken elsewhere on the board.

b. Minimize the distance (less than 0.25 in, or 6.35 mm) from the power-supply pins to high-frequency 0.1-µF decoupling capacitors. At the device pins, the ground and power plane layout must not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections must always be decoupled with these capacitors. An optional supply decoupling capacitor across the two power supplies (for bipolar operation) improves second-harmonic distortion performance. Larger (2.2 µF to 6.8 µF) decoupling capacitors, effective at lower frequencies, must also be used on the main supply pins. These capacitors can be placed somewhat farther from the device and can be shared among several devices in the same area of the PCB.

c. Careful selection and placement of external components preserve the high-frequency performance of the THS6212. Resistors must be of a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal film and carbon composition, axially-leaded resistors can also provide good high-frequency performance.

   Again, keep leads and PCB trace length as short as possible. Never use wire-wound type resistors in a high-frequency application. Although the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, must also be placed close to the package. Where double-side component mounting is allowed, place the feedback resistor directly under the package on the other side of the board between the output and inverting input pins. The frequency response is primarily determined by the feedback resistor value as described in the wideband current-feedback operation *Detailed Design Procedure* section. Increasing the value reduces the bandwidth, whereas decreasing the value leads to a more peaked frequency response. The 1.24-kΩ feedback resistor used in the *Typical Characteristics* sections at a gain of 10 V/V on ±12-V supplies is a good starting point for design. Note that a 1.5-kΩ feedback resistor, rather than a direct short, is recommended for a unity-gain follower application. A current-feedback op amp requires a feedback resistor to control stability even in the unity-gain follower configuration.

d. Connections to other wideband devices on the board can be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 mils to 100 mils [0.050 in to 0.100 in, or 1.27 mm to 2.54 mm]) must be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the recommended R_S versus capacitive load plots (see Figure 5, Figure 23, Figure 35, Figure 47, Figure 60, and Figure 72). Low parasitic capacitive loads (less than 5 pF) may not need an isolation resistor because the THS6212 is nominally compensated to operate with a 2-pF parasitic load. If a long trace is required, and the 6-dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched-impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50-Ω environment is not necessary on board; in fact, a higher impedance environment improves distortion (see the distortion versus load plots). With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the THS6212 is used, as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device.

   This total effective impedance must be set to match the trace impedance. The high output voltage and current capability of the THS6212 allows multiple destination devices to be handled as separate transmission lines, each with their own series and shunt terminations. If the 6-dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only.

Layout Guidelines (continued)

Treat the trace as a capacitive load in this case and set the series resistor value as shown in the recommended R_S versus capacitive load plots. However, this configuration does not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there is some signal attenuation as a result of the voltage divider formed by the series output into the terminating impedance.

e. Socketing a high-speed part such as the THS6212 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network, and can make achieving a smooth, stable frequency response almost impossible. Best results are obtained by soldering the THS6212 directly onto the board.

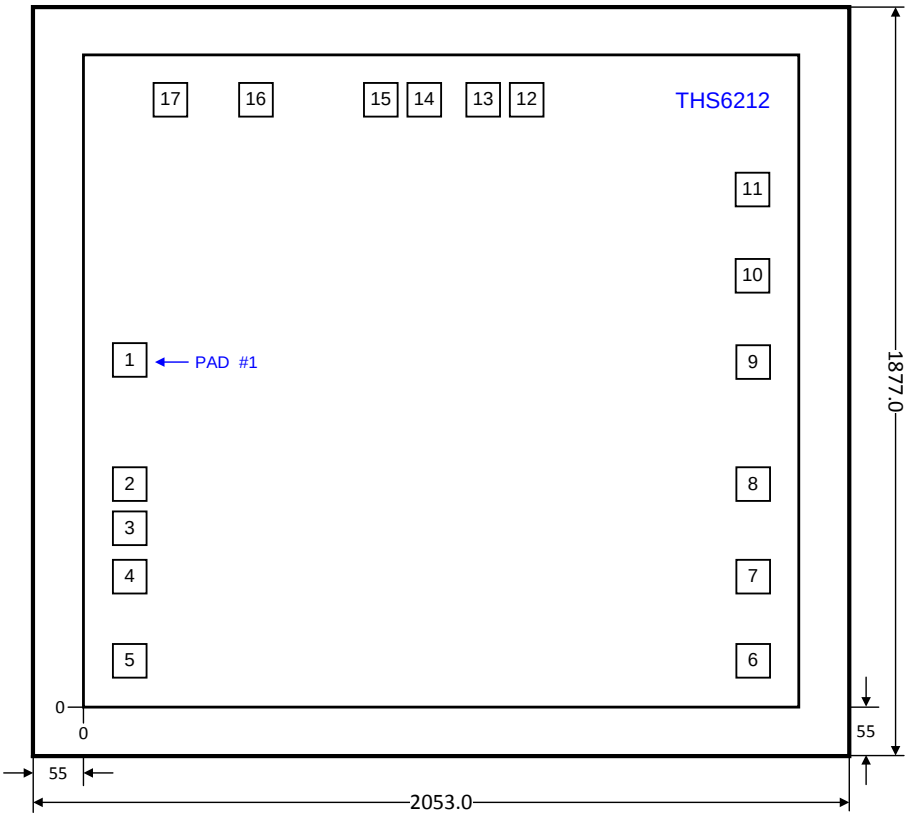
f. Use the $-V_S$ plane to conduct heat out of the package. The package attaches the die directly to an exposed thermal pad on the bottom, and must be soldered to the board. This pad must be connected electrically to the same voltage plane as the most negative supply applied to the THS6212 (in Figure 84, this supply is –12 V).

10.2 Wafer and Die Information

Table 3 lists wafer and bond pad information for the YS package.

Table 3. Wafer and Bond Pad Information

WAFER BACKSIDE FINISH	WAFER THICKNESS	BACKSIDE POTENTIAL	BOND PAD METALLIZATION	BOND PAD DIMENSIONS (X × Y)
Silicon without backgrind	25 mils	Floating or any potential inclusive of and in between V_{S+} and V_{S-} (must be thermally dissipative)	AlCu	101.60 µm × 101.60 µm



NOTE: All dimensions are in micrometers (µm).

Figure 89. Die Dimensions

Table 4 lists the bond pad locations for the YS package. All dimensions are in micrometers (µm).

Table 4. Bond Pad Locations

PAD NUMBER	PAD NAME	X MIN	Y MIN	X MAX	Y MAX	DESCRIPTION
1	D1_IN+	23.50	888.20	125.10	989.80	Amplifier D1 noninverting input
2	D2_IN+	23.50	534.20	125.10	635.80	Amplifier D2 noninverting input
3	DNB	23.50	404.20	125.10	505.80	Do not bond (for internal use)
4	GND	23.50	267.50	125.10	369.10	Control pin ground reference
5	IADJ	23.50	23.50	125.10	125.10	Bias current adjustment pin
6	D2_OUT (OPT)	1817.9	36.20	1919.50	137.80	Optional amplifier D2 output (can be left unconnected or connected to pad 7)
7	D2_OUT	1817.9	282.80	1919.50	384.40	Amplifier D2 output (must be used for D2 output)
8	D2_FB	1817.9	534.20	1919.50	635.80	Amplifier D2 inverting input
9	D1_FB	1817.9	888.20	1919.50	989.80	Amplifier D1 inverting input
10	D1_OUT	1817.9	1139.60	1919.50	1241.20	Amplifier D1 output (must be used for D1 output)
11	D1_OUT (OPT)	1817.9	1386.20	1919.50	1487.80	Optional amplifier D1 output (pad can be left unconnected or connected to pad 10)
12	VS+	1171.40	1641.90	1273.00	1743.50	Positive power-supply connection
13	VS+	1041.40	1641.90	1143.00	1743.50	Positive power-supply connection
14	VS–	873.60	1641.90	975.20	1743.50	Negative power-supply connection
15	VS–	743.60	1641.90	845.20	1743.50	Negative power-supply connection
16	BIAS-1	393.60	1641.90	495.20	1743.50	Bias mode parallel control, LSB
17	BIAS-2	143.60	1641.90	245.20	1743.50	Bias mode parallel control, MSB

10.3 Layout Example

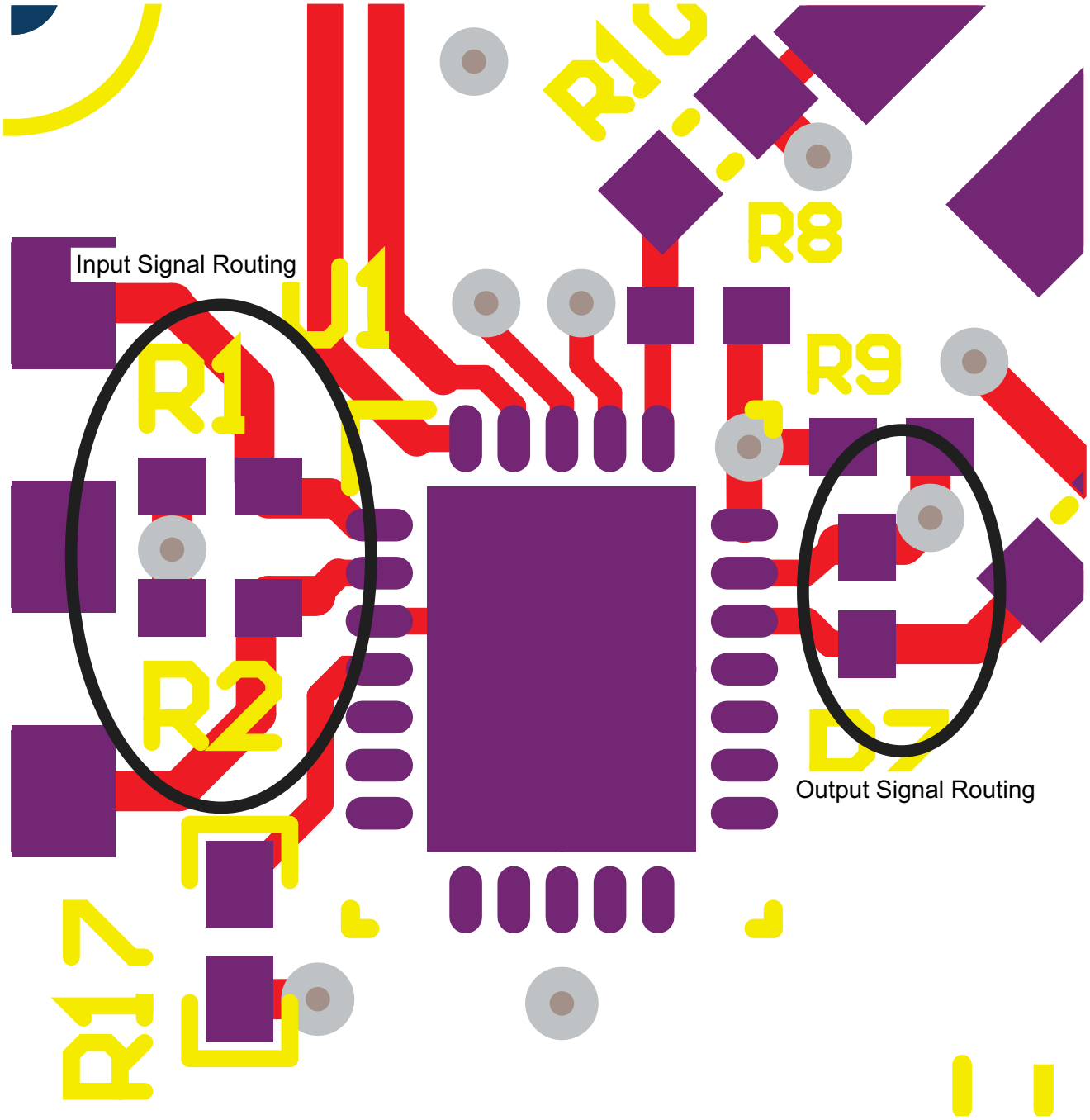


Figure 90. THS6212EVM Top Layer Example

Layout Example (continued)

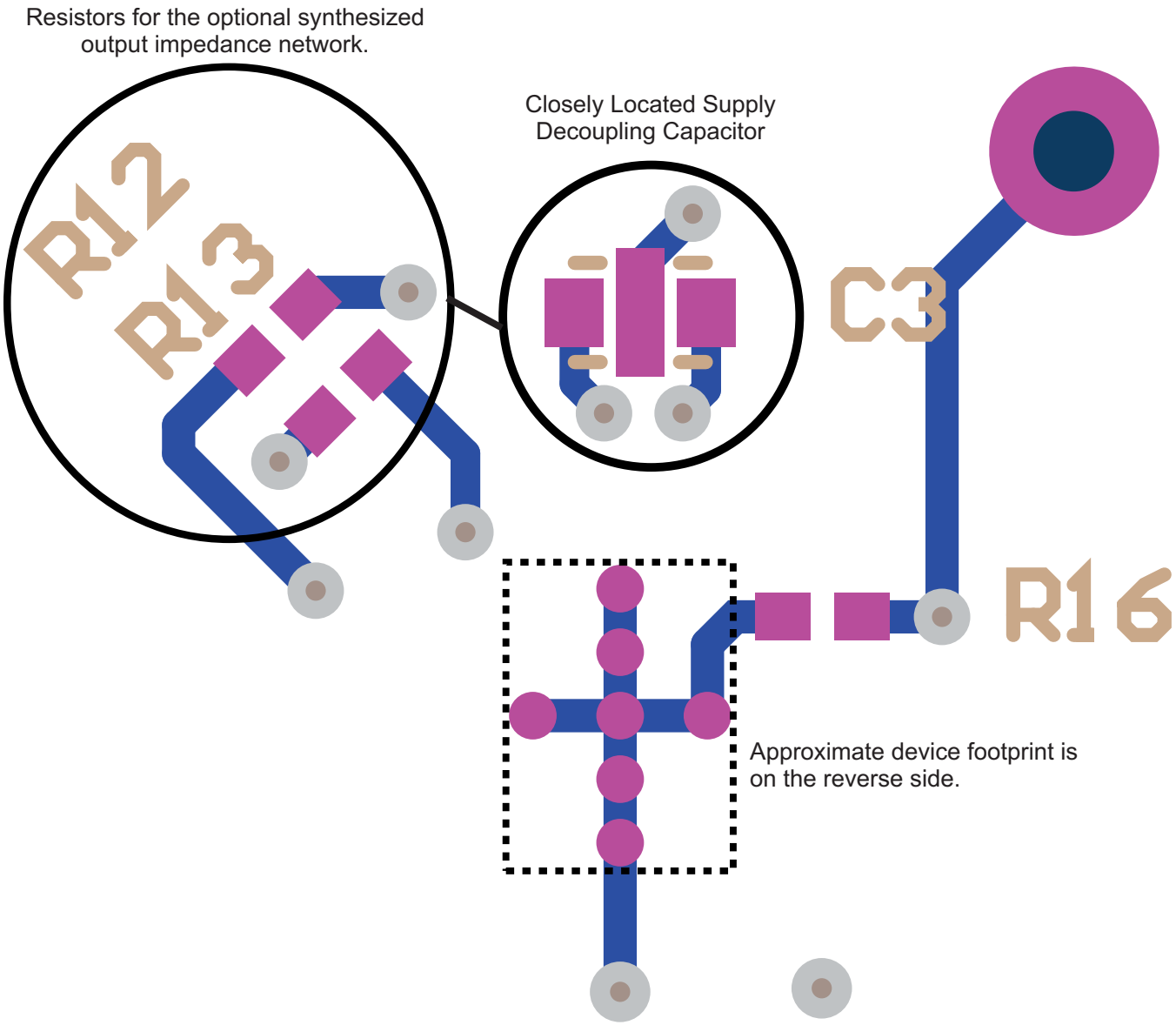


Figure 91. THS6212EVM Bottom Layer Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

THS6214 Dual-Port, Differential, VDSL2 Line Driver Amplifiers

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS6212IRHFR	ACTIVE	VQFN	RHF	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	THS6212	Samples
THS6212IRHFT	ACTIVE	VQFN	RHF	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	THS6212	Samples
THS6212YS	ACTIVE	WAFERSALE	YS	0	1	TBD	Call TI	Call TI			Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

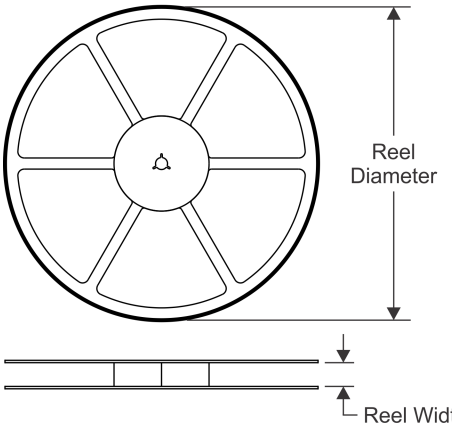
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

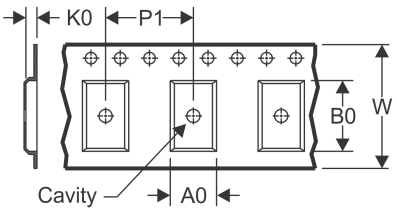
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

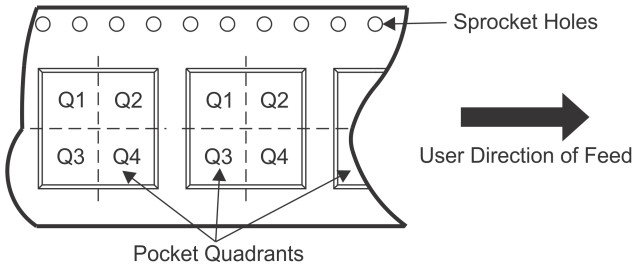


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

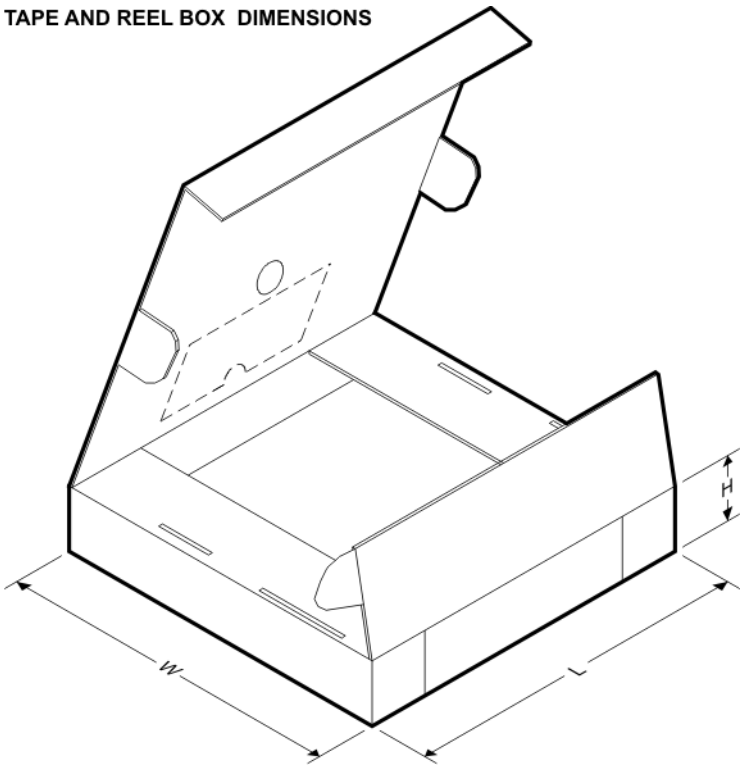
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS6212IRHFR	VQFN	RHF	24	3000	330.0	12.4	4.3	5.3	1.1	8.0	12.0	Q1
THS6212IRHFR	VQFN	RHF	24	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
THS6212IRHFT	VQFN	RHF	24	250	180.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
THS6212IRHFT	VQFN	RHF	24	250	180.0	12.5	4.3	5.3	1.1	8.0	12.0	Q1

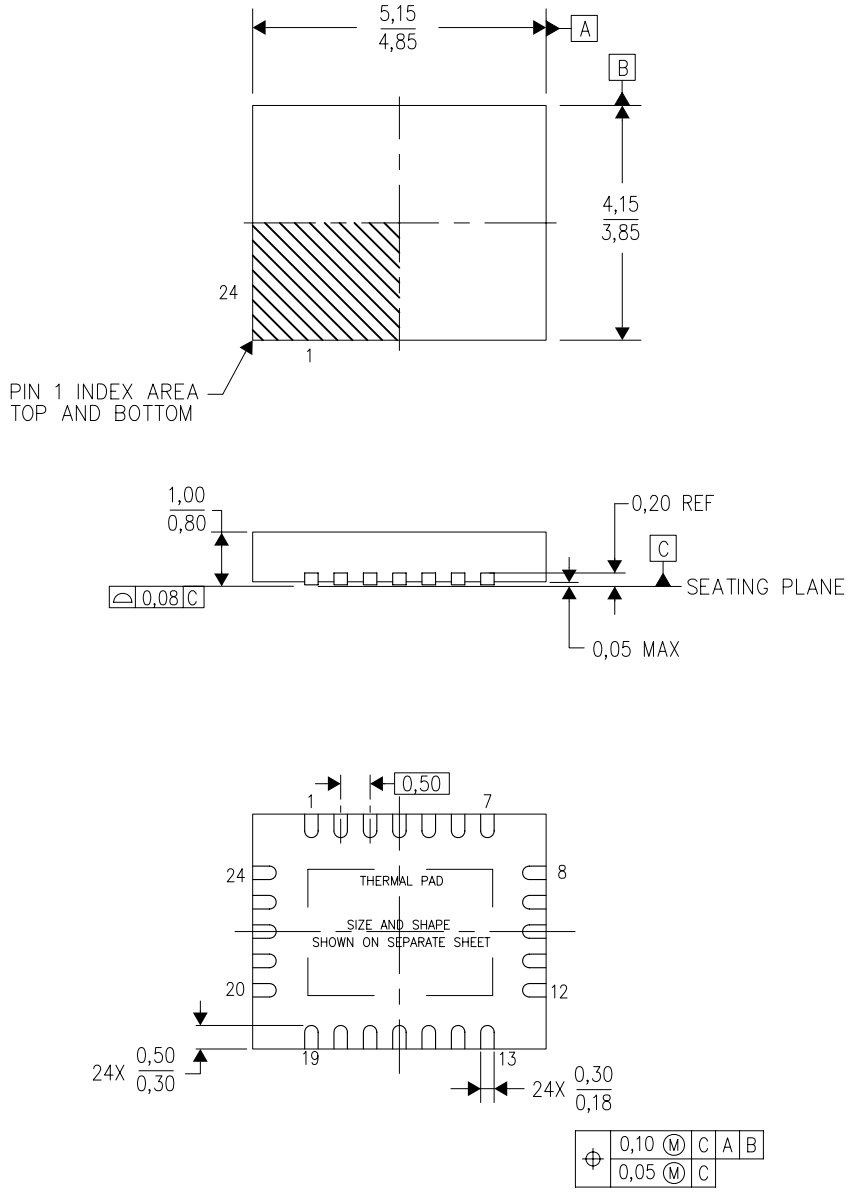
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS6212IRHFR	VQFN	RHF	24	3000	338.0	355.0	50.0
THS6212IRHFR	VQFN	RHF	24	3000	367.0	367.0	35.0
THS6212IRHFT	VQFN	RHF	24	250	210.0	185.0	35.0
THS6212IRHFT	VQFN	RHF	24	250	205.0	200.0	33.0

RHF (R–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



4204845–2/H 06/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

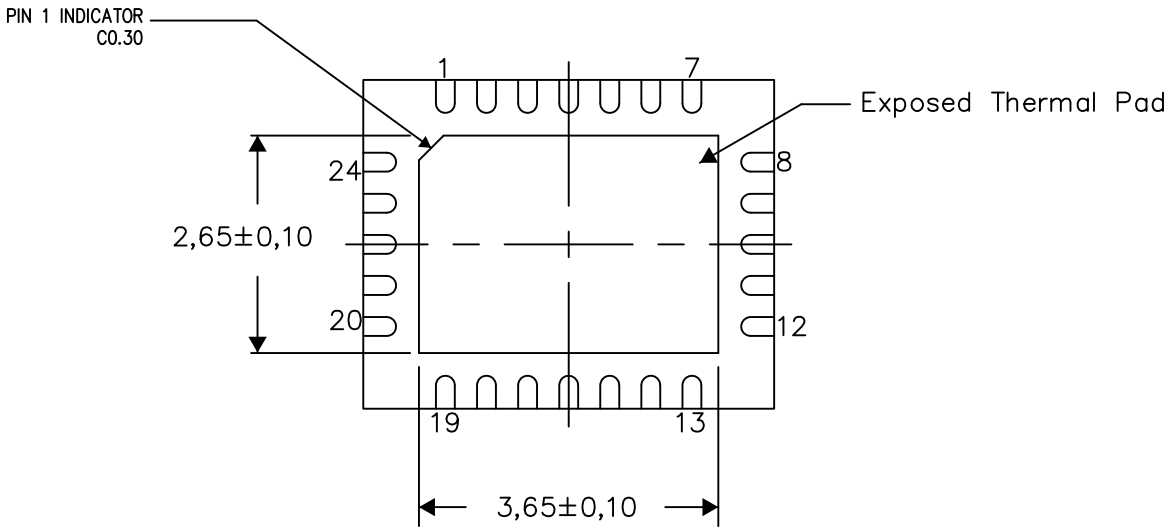
RHF (R–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



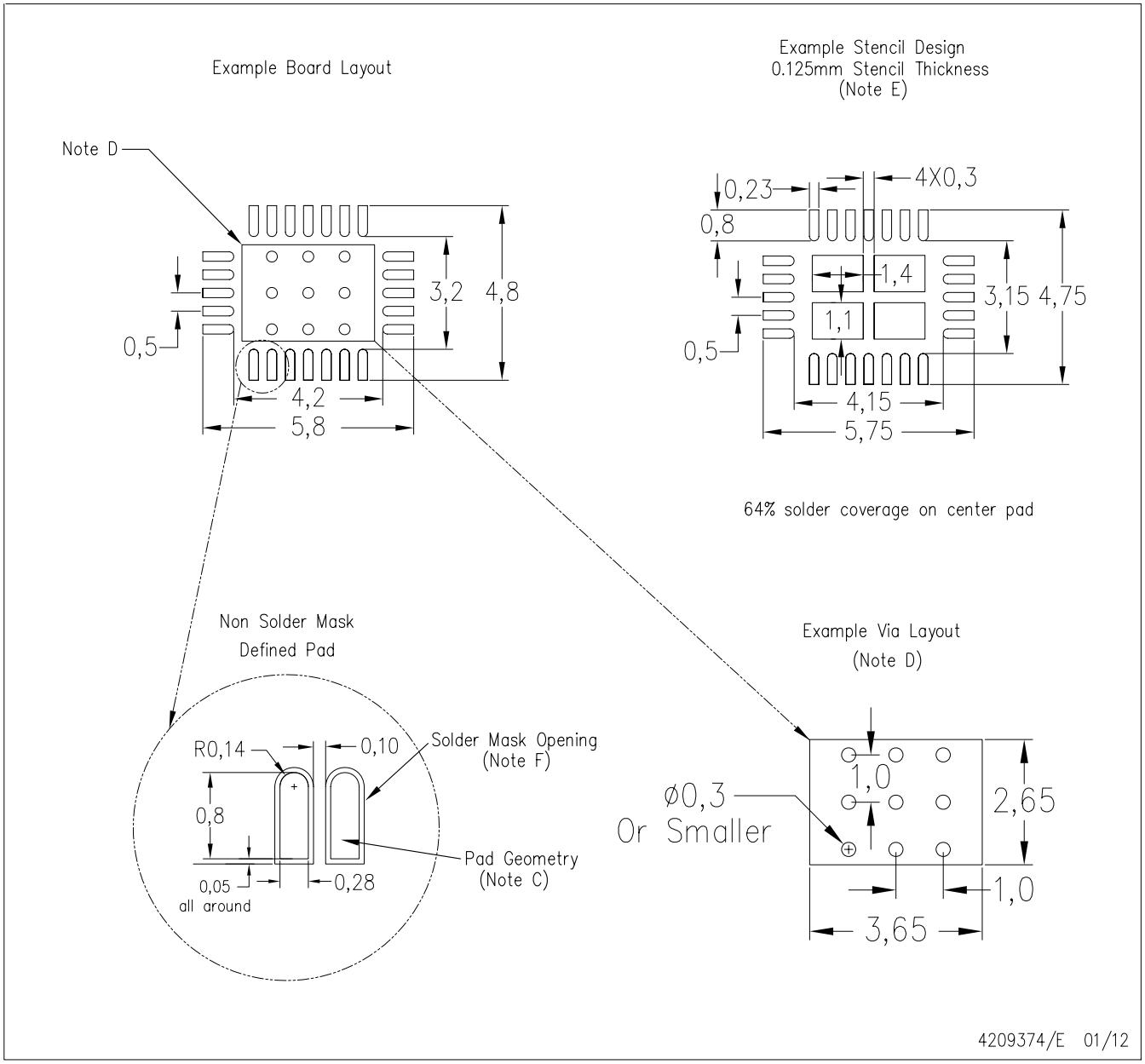
Bottom View

Exposed Thermal Pad Dimensions

4206360–3/K 02/14

NOTE: All linear dimensions are in millimeters

RHF (R–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265