

# FDMS4D0N12C

## Power MOSFET

120 V, 4.0 mΩ, 118 A, Single N-Channel, PQFN56

### Features

- Small Footprint (5x6 mm) for Compact Design
- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low  $Q_G$  and Capacitance to Minimize Driver Losses
- These are Pb-free, Halogen Free / BFR Free and are RoHS Compliant

### Typical Applications

- Synchronous Rectification
- AC-DC and DC-DC Power Supplies
- AC-DC Adapters (USB PD) SR
- Load Switch

### MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ , Unless otherwise specified)

Parameter		Symbol	Value	Unit	
Drain-to-Source Voltage		$V_{DS}$	120	V	
Gate-to-Source Voltage		$V_{GS}$	$\pm 20$	V	
Continuous Drain Current $R_{\theta JC}$ (Note 7)	Steady State	$T_C = 25^\circ\text{C}$	$I_D$	114	A
			$P_D$	106	W
Continuous Drain Current $R_{\theta JA}$ (Note 6, 7)	Steady State	$T_A = 25^\circ\text{C}$	$I_D$	18.5	A
			$P_D$	2.7	W
Pulsed Drain Current	$T_A = 25^\circ\text{C}$ , $t_p = 10 \mu\text{s}$	$I_{DM}$	628	A	
Operating Junction and Storage Temperature		$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$	
Source Current (Body Diode)		$I_S$	114	A	
Single Pulse Drain-to-Source Avalanche Energy ( $I_{AV} = 66.7 \text{ A}$ , $L = 0.1 \text{ mH}$ )		$E_{AS}$	222	mJ	
Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from case for 10 s)		$T_L$	300	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

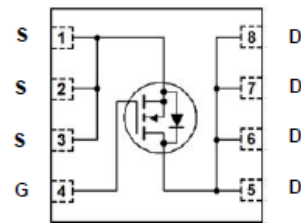


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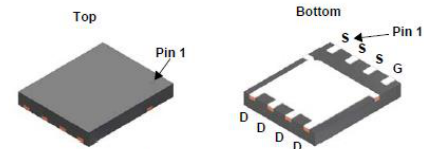
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$V_{(BR)DDS}$	$I_D \text{ MAX}$	$R_{DS(on)} \text{ MAX}$
120 V	67 A	4.0 mΩ @ 10 V
	33 A	8.0 mΩ @ 6 V

### ELECTRICAL CONNECTION

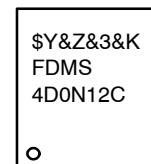


N-Channel MOSFET



Power 56  
(PQFN8 5x6)  
CASE 483AF

### MARKING DIAGRAM



$\$Y$  = ON Semiconductor Logo  
 $\&Z$  = Assembly Plant Code  
 $\&3$  = Numeric Date Code  
 $\&K$  = Lot Code  
 FDMS4D0N12C = Specific Device Code

### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

# FDMS4D0N12C

## ORDERING INFORMATION

Device	Package	Shipping†
FDMS4D0N12C	PQFN8 (Power 56) (Pb-Free)	3,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

## THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction – to – Case – Steady State (Note 7)	$R_{\theta JC}$	1.18	°C/W
Junction – to – Ambient – Steady State (Note 7)	$R_{\theta JA}$	45	

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain – to – Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	120			V
Drain – to – Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = 250\ \mu\text{A}$ , ref to $25^\circ\text{C}$		49		mV/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 96\text{ V}$	$T_J = 25^\circ\text{C}$		1	$\mu\text{A}$
			$T_J = 125^\circ\text{C}$		100	$\mu\text{A}$
Gate – to – Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA

### ON CHARACTERISTICS (Note 8)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 370\ \mu\text{A}$	2.0		4.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	$I_D = 370\ \mu\text{A}$ , ref to $25^\circ\text{C}$		-8.5		mV/°C
Drain – to – Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 67\text{ A}$		3.3	4.0	m $\Omega$
		$V_{GS} = 6\text{ V}, I_D = 33\text{ A}$		4.7	8.0	
Forward Transconductance	$g_{FS}$	$V_{DS} = 5\text{ V}, I_D = 67\text{ A}$		144		S
Gate-Resistance	$R_G$	$T_A = 25^\circ\text{C}$		0.9	1.8	$\Omega$

### CHARGES & CAPACITANCES

Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 60\text{ V}$		4565	6460	pF	
Output Capacitance	$C_{OSS}$			2045	3060		
Reverse Transfer Capacitance	$C_{RSS}$			17	24		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 6\text{ V}, V_{DS} = 60\text{ V}, I_D = 67\text{ A}$		36	51	nC	
Total Gate Charge	$Q_{G(TOT)}$		$V_{GS} = 10\text{ V}, V_{DS} = 60\text{ V}, I_D = 67\text{ A}$		58		82
Gate-to-Source Charge	$Q_{GS}$				21		
Gate-to-Drain Charge	$Q_{GD}$				9		
Plateau Voltage	$V_{GP}$			5		V	
Output Charge	$Q_{OSS}$	$V_{DD} = 60\text{ V}, V_{GS} = 0\text{ V}$		207		nC	

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## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### SWITCHING CHARACTERISTICS (Note 8)

Turn – On Delay Time	t <sub>d(ON)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 60 V, I <sub>D</sub> = 67 A, R <sub>G</sub> = 6 Ω		25	41	ns
Rise Time	t <sub>r</sub>			8	16	
Turn – Off Delay Time	t <sub>d(OFF)</sub>			45	72	
Fall Time	t <sub>f</sub>			12	22	

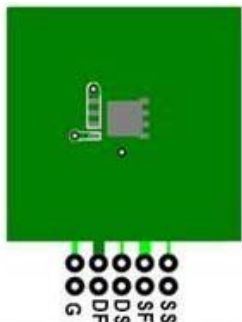
### DRAIN–SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 67 A	T <sub>J</sub> = 25°C		0.86	1.3	V
			T <sub>J</sub> = 125°C		0.7	1.2	
Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = 0 V, dI <sub>S</sub> /dt = 300 A/μs, I <sub>S</sub> = 33 A			53	84	ns
Reverse Recovery Charge	Q <sub>RR</sub>				175	280	nC
Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = 0 V, dI <sub>S</sub> /dt = 1000 A/μs, I <sub>S</sub> = 33 A			36	57	ns
Reverse Recovery Charge	Q <sub>RR</sub>				360	575	nC

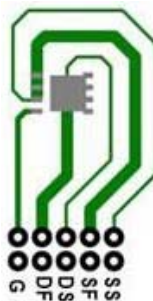
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

#### NOTES:

- R<sub>θJA</sub> is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR-4 material. R<sub>θCA</sub> is determined by the user's board design.



- a) 45°C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



- b) 115°C/W when mounted on a minimum pad of 2 oz copper.

- Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
- E<sub>AS</sub> of 222 mJ is based on starting T<sub>J</sub> = 25°C; L = 0.1 mH, I<sub>AS</sub> = 66.7 A, V<sub>DD</sub> = 100 V, V<sub>GS</sub> = 12 V, 100% tested at L = 0.1 mH, I<sub>AS</sub> = 66.7 A.
- Pulsed I<sub>D</sub> please refer to Fig. 11 SOA graph for more details.
- Computed continuous current limited to max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.
- Surface-mounted on FR4 board using 1 in<sup>2</sup> pad size, 2 oz Cu pad.
- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- Switching characteristics are independent of operating junction temperatures.

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## TYPICAL CHARACTERISTICS

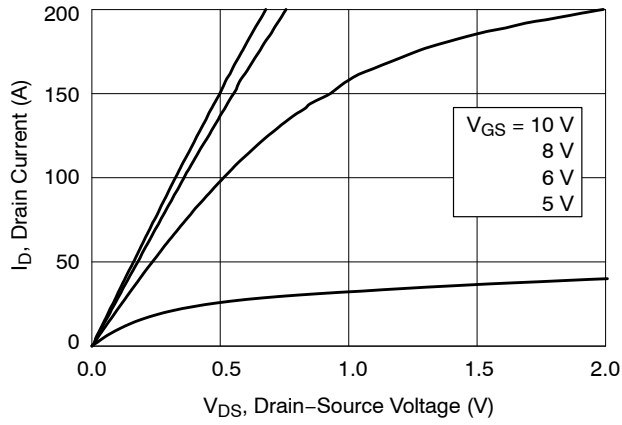


Figure 1. On-Region Characteristics

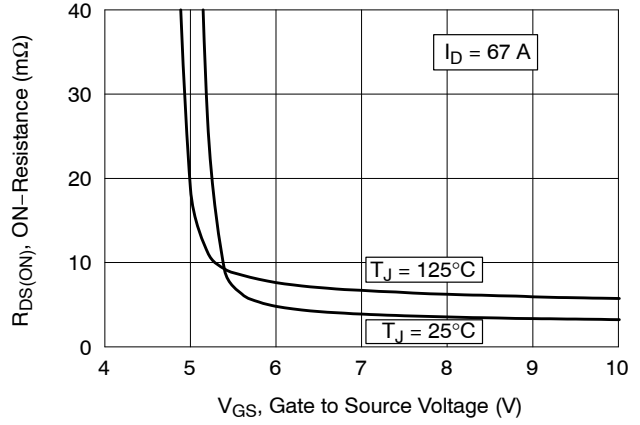


Figure 2. Transfer Characteristics

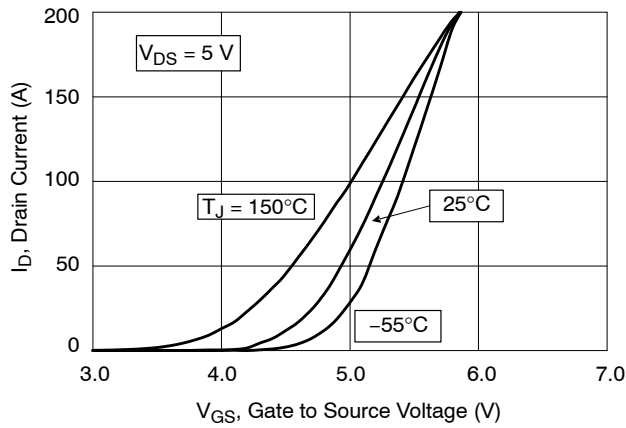


Figure 3. On-Resistance vs. Gate-to-Source Voltage

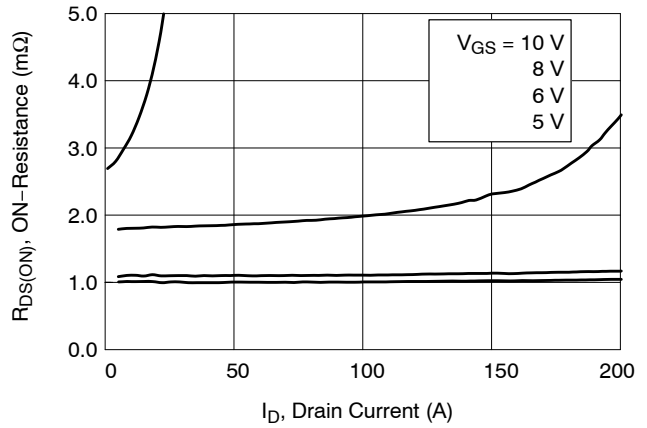


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

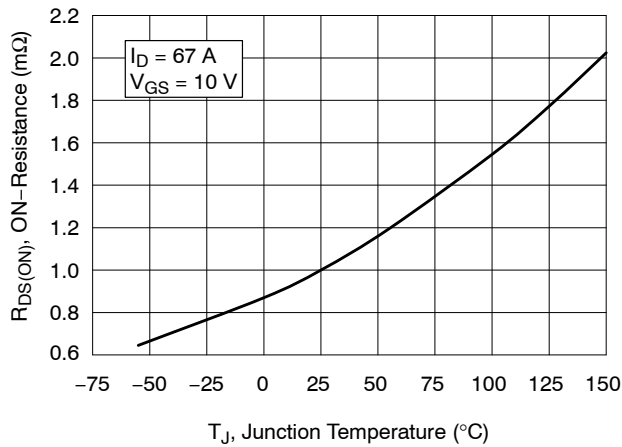


Figure 5. On-Resistance Variation with Temperature

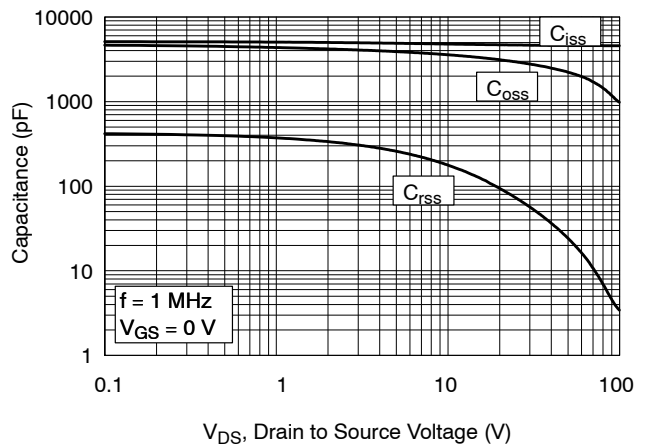


Figure 6. Capacitance Variation

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## TYPICAL CHARACTERISTICS (continued)

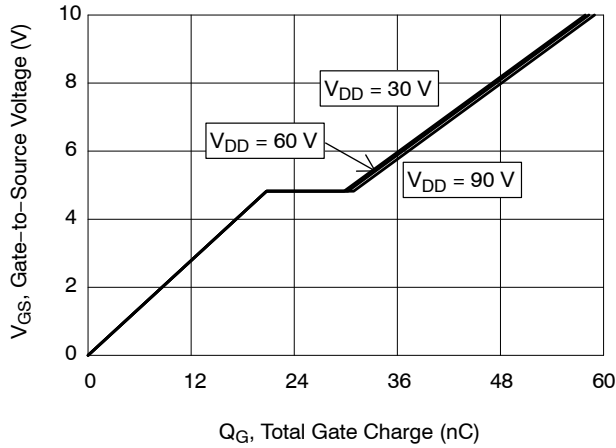


Figure 7. Gate-to-Source Voltage vs. Total Charge

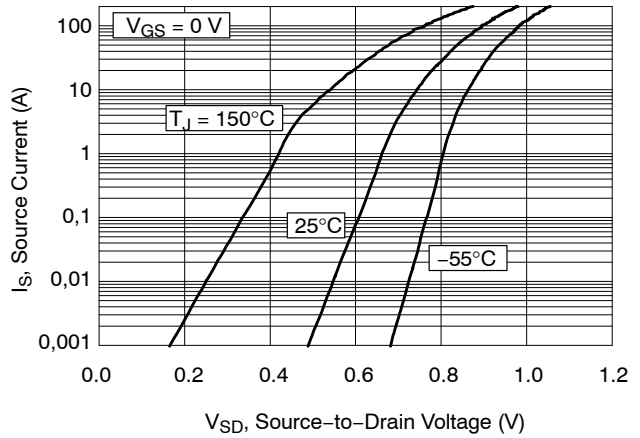


Figure 8. Diode Forward Voltage vs. Current

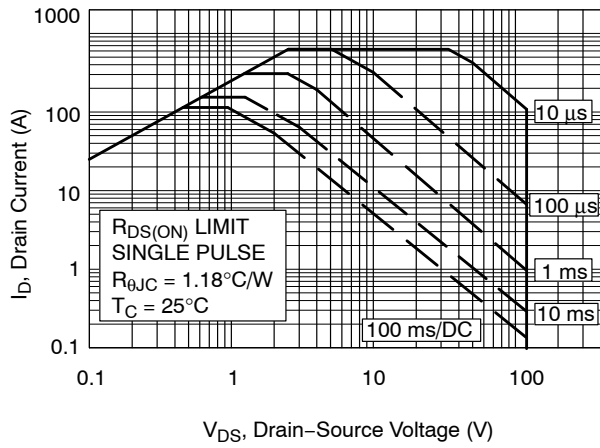


Figure 9. Safe Operating Area

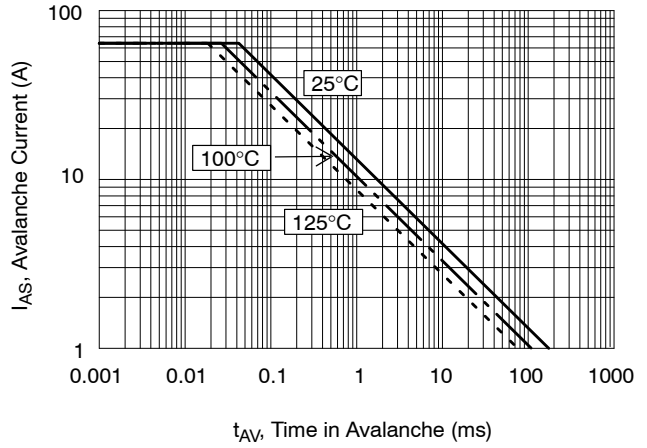


Figure 10.  $I_{PEAK}$  vs. Time in Avalanche

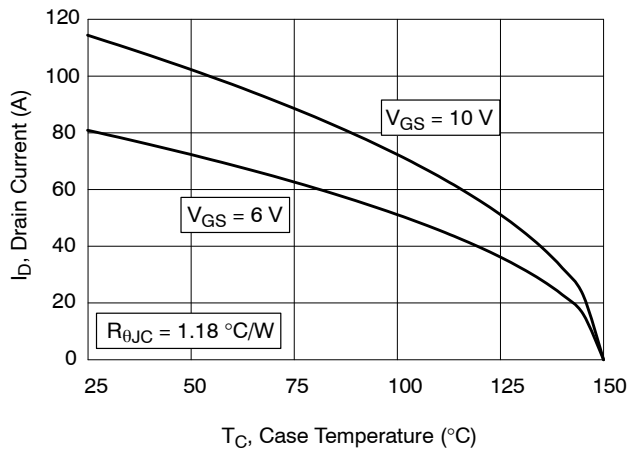


Figure 11. Maximum Drain Current vs. Case Temperature

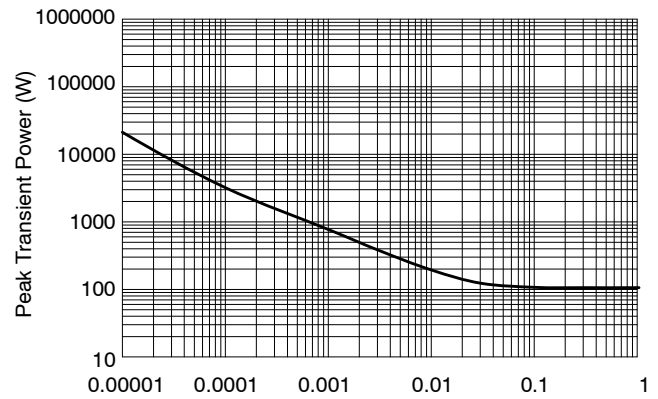


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (continued)

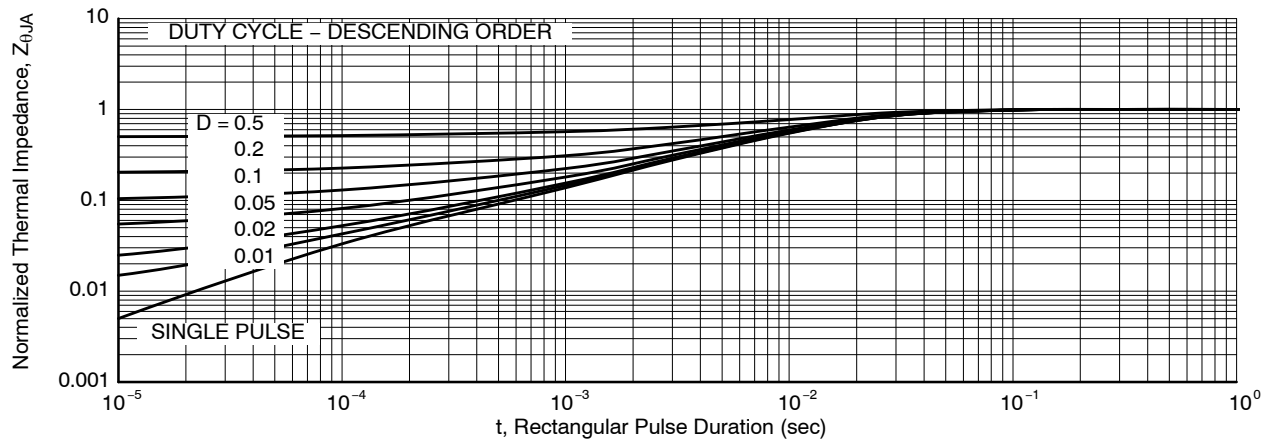
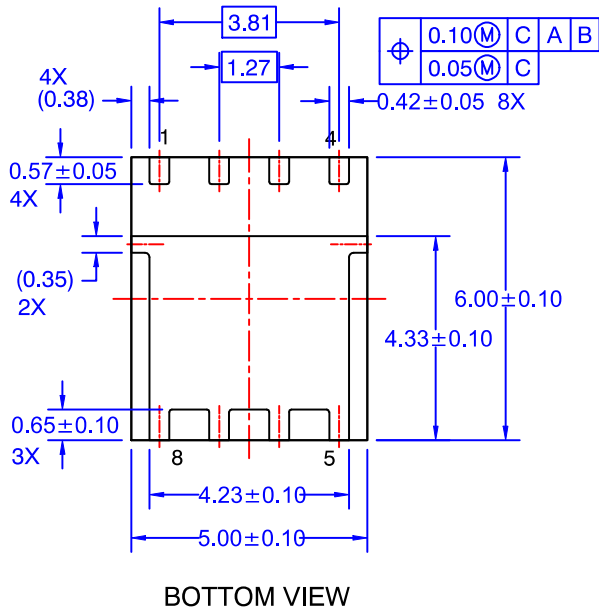
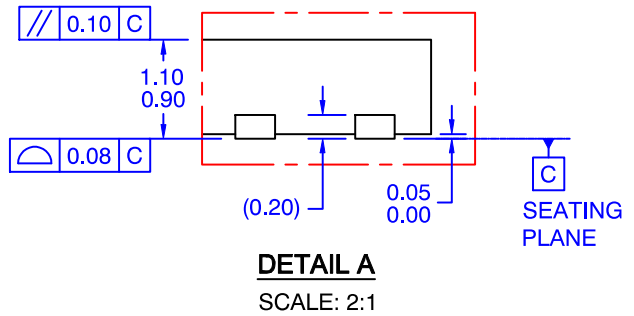
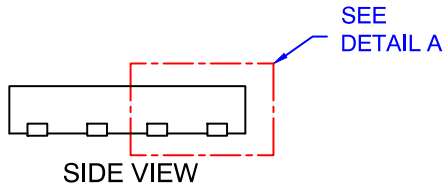
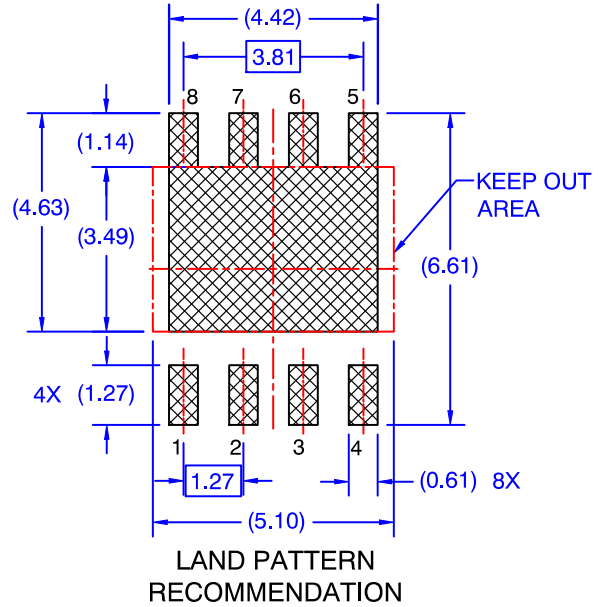
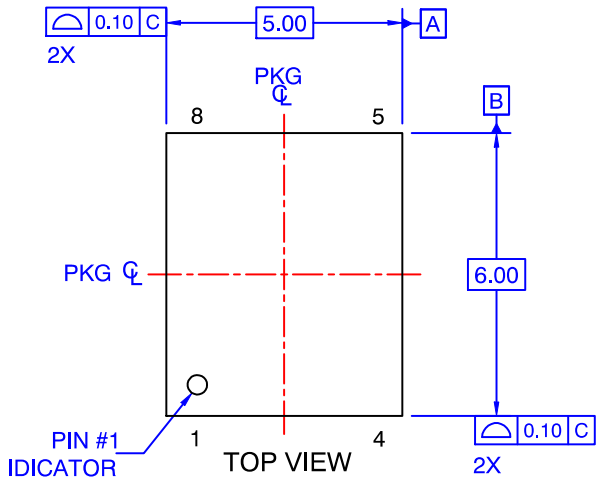


Figure 13. Transient Thermal Response Curve


# FDMS4D0N12C

## PACKAGE DIMENSIONS

PQFN8 5X6, 1.27P  
CASE 483AF  
ISSUE O



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA,
  - B) ALL DIMENSIONS ARE IN MILLIMETERS.
  - C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
  - D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
  - E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

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